The T-lam System

T-guide for Performance

Part I: Design Guidelines for Performance & Reliability with Thermagon IMpcb and 1KA Dielectric

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Part I: Design Guidelines for Performance & Reliability with Thermagon IMpcb and 1KA Dielectric

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The Insulated Metal Printed Circuit Board (IMpcb) can replace Standard FR4 Boards or Ceramic Substrates in Power or Thermal applications. The IMpcb type materials are also known as IMST (Insulated Metal Substrate Technology), MCS (Metal Core Substrate), Hitt Plate and IMS (Insulated Metal Substrate). The technology was developed in Japan in the late 1970s as IMST, and now is used extensively in high volume commercial and industrial products including power amplifiers, power supplies, motor controllers, HV TV deflection, UPS, battery chargers, welders, and more.

The basic construction is a thin dielectric layer, between copper foil tracks and a metal base plate. The primary technology is in the dielectric material, which must provide good thermal conductivity and good dielectric isolation. The Thermagon T-preg dielectric uses a superior thermal filler, which provides the exceptional thermal performance without making the dielectric too thin, and without excessive filler content. As a result, the T-preg has many other secondary electrical and mechanical advantages over alternate materials.

Power Electronic Products today are being required to provide more performance, in less space, and at lower costs. As a result, the PCB or substrate must provide improved electrical, thermal and mechanical performance. To meet these needs, designers must have the same electrical, thermal and mechanical information, which would be expected with any electrical component. Thermagon provides this type of information in Data Sheets, Design Guidelines and Computer Models. The information allows the designer to plan and optimize for performance, reliability, manufacturability and low cost, using the Thermagon IMpcb products. The IMpcb typically simplifies the system architecture, resulting in performance, size, reliability and cost advantages, which extend beyond the substrate or board.

The T-guide, Part I: Design Guidelines for Performance was developed first, so that the user can capitalize on the unique performance advantages of the Thermagon IMpcb materials. Additional design aids will be available in early 2000, and they will include:

a) Electronic Computer Performance Models for all data in the Performance Design Guidelines, which will operate on Microsoft Excel software.
b) T-guide, Part II: Manufacturing Design Guideline with design information for manufacturability including recommended dimensions, tolerances, materials and process, and suggestions for lowest cost system design.

Most of this information is available informally on request today, so call Thermagon for application support with performance, reliability and manufacturability questions.

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1.0 **Thermal Properties**

The primary advantage of the IMpcb technology is improved thermal performance, while retaining good dielectric isolation at low cost. The Thermagon IMpcb uses the highest thermally conductive filler systems in this industry, which minimizes filler content and maintains the integrity of the dielectric layer. In designing with the IMpcb, it is important to capitalize on the thermal advantages, without adding unnecessary complexity or costs. Thermal advantages can reduce component size, track width, thermal and mechanical hardware, and electrical & thermal interconnects.

1.1 Thermal Conductivity of the T-preg Dielectric

The Thermagon 1KA T-preg dielectric has a thermal conductivity of 3.0 W/mC° (0.076 W/in.C°) in the vertical direction, and greater than 5.0 W/mC° (0.127 W/in.C°) in the lateral direction. The following design information is based on the vertical thermal conductivity value, but there are PCB type applications that can take additional advantages of the higher lateral thermal conductivity. The improved thermal conductivity has both direct and indirect advantages including:

1.1.1 Improved heat transfer from components, which can improve reliability, reduce component size/cost, eliminate component heat sinks & hardware, reduce PCB/substrate size and/or increase product density.

1.1.2 Higher current density in traces, vias and connectors are possible, because the IMpcb removes the heat and lowers the temperature. Standard PCB current density rules are limited by temperature rise, and using the PCB rules for IMpcb will unnecessarily increase the size and cost of your product.

1.2 Thermal Resistance of the IMpcb

The thermal resistance of the dielectric layer is a function of the dielectric thermal conductivity and thickness, and of the area of the power component or pad. The thermal resistance of the IMpcb is defined as:

$R(°) = t/\sigma A$, where

$R(°)$ = Thermal Resistance (C°/W)
t = Dielectric Thickness (inch)
σ = Thermal Conductivity (W/in.C°)
A = Area (square inch)

The Thermal Resistance versus Dielectric Thickness for the 1KA T-preg is shown in Figure 1.1a per square inch and in Figure 1.1b per square centimeter. The thermal resistance is shown below for select dielectric thicknesses:

Dielectric Thickness (inches/microns)	Thermal Resistance (C°/W per sq.in.)	Thermal Resistance (C°/W per sq.cm.)
0.004/102	0.052	0.339
0.006/152	0.079	0.508
0.008/203	0.105	0.677
0.010/254	0.131	0.847

The given thermal resistance is based on an infinite plane. In real applications the pad and tracks are small, and there is an edge or heat spreading effect, which reduces the thermal resistance further by transferring heat over an effective larger area of the dielectric. The thermal resistance versus dielectric thickness for a number of pad sizes is shown in Figure 1.2. The thermal resistance values were calculated based on 2 oz copper foil, 0.004" to 0.020" thick dielectric, and 1/16" (0.062") aluminum base plate. The thermal resistance of some select pad sizes and dielectric thickness are shown below:

Dielectric Thickness	Thermal Resistance (C8/W) for Pad Sizes of: 0.2"x0.2"	0.4"x0.4"	0.8"x0.8"	1.0"x1.0"
0.004"	1.45	0.38	0.094	0.064
0.006"	2.04	0.54	0.134	0.089
0.008"	2.61	0.69	0.178	0.115
0.010"	3.15	0.84	0.217	0.140
0.012"	3.68	0.99	0.256	0.165
0.020"	5.59	1.55	0.408	0.264

1.3 Thermal and Power Management

The IMpcb is rated @ 1308C continuous operation, and recognized by UL for that temperature. The peak or maximum temperatures can be as high as 2608C for 30 seconds, during solder reflow, but repetitive peak application temperatures are not recommended above 1758C. In continuous or steady state operation, the maximum power of a component or trace is limited by the 1308C maximum temperature at the dielectric to copper foil interface.

$P(max) = \Delta T_{FB}/R(Y)_{FB}$, where P(max) = Maximum Power Dissipation (watts),
$\Delta T_{FB} = t_F - t_B$, t_F = Foil Temp.(8C), t_B = Base Temp.(8C),
$R(Y)_{FB}$ = Thermal Resistance F to B (8C/watt).

The Base Plate temperature is a function of the total IMpcb power dissipated, and the thermal resistance between the base plate and ambient, which is defined as follows:

$P(IMpcb) = \Delta T_{BA}/R(Y)_{BA}$, where P(IMpcb) = Total Power Dissipation on IMpcb (watts)
$\Delta T_{BA} = t_B - t_A$; t_A = Ambient Temperature (8C)
$R(Y)_{BA}$ = Thermal Resistance Base to Ambient (C8/watt)

The heat transfer from base plate to ambient will vary with application, power levels, ambient temperature, etc. The base plate can be cooled with natural or forced convection, or by conduction to a heat sink, bracket or other mounting surface.

In Medium Power Applications, the ambient air may provide sufficient heat removal from the IMpcb. The rule of thumb is $R(Y)_{BA}$ = 508C/W per square inch of IMpcb surface (each sides), in natural convection. The ΔT can be reduced significantly with forced convection. A $R(Y)_{BA}$ of 15-25 8C/W per square inch may be typical, but can vary significantly with airflow, component contour, etc. Any estimated ΔT_{BA} should be confirmed with Thermal Finite Element Analysis (FEA) and/or actual measurements.

In High Power Applications or Power Modules, the heat is typically transferred by conduction to a heat sink or metal mounting surface. The temperature of that surface may be known, or can be calculated as a function of power dissipation, size, shape, ambient temperature, and air flow. These parameters are application specific, and Thermagon can provide application assistance for your special application.

Thermagon also offers a broad range of high performance thermal interface materials, which can be used between the IMpcb and the mounting surface. These include Thermal Elastomers (T-pli 200), Thermal Grease and Adhesives (T-gon 100, 200, 300 & 400), Thermal Pads (T-flex 200), and Thermal Putty (T-putty 500). Contact Thermagon for detailed information and literature on these products.

The Maximum Thermal Resistance values provided are calculated, and design guard-bands are recommended. The actual guard-band will be application specific, although a 15-25% is typical. If your application or device is insensitive to short times above maximum rated temperatures, a 15% guard-band may be adequate. If you have a device that is thermally sensitive, or that may go into thermal run-away above the maximum rated temperature, you may need a 25% or larger guard-band.

Finally, these are thermal resistance for given areas. The actual thermal resistance can be reduced significantly with special techniques including thicker copper, solderable heat spreaders, inner-layers and thermal vias. Thermagon will work with you to optimize your specific product or application.

2.0 Dielectric Isolation

The dielectric strength or dielectric isolation voltage is a measure of the IMpcb dielectric's ability to withstand high voltages between copper foil and base plate on single sided substrates, as well as between foil layers on multi-layer substrates and DSL (Double Sided Layer) boards.

2.1 Hipot Testing

The dielectric strength is measured using a Hipot or High Potential Test. This test applies a high voltage for a given time, and the dielectric must not breakdown. Most products worldwide are tested and/or recognized per Underwriters Laboratory (UL) conditions and limits. Most other regulatory agents have equivalent or similar requirements. Important exceptions, which may apply are special EC transient tests and VDE partial discharge tests.

The UL test limits and conditions can be quite complex, because they are application specific, but the majority of the applications for IMpcb can be covered by some select UL test and conditions for Power Conversion Equipment. These conditions and limits are given below, as a measure of the Dielectric Strength of the Thermagon T-preg, and as a guideline for typical applications. If your product must comply with any of these agencies, the applicable UL, EC, VDE, CSA or other specification should be consulted.

Application Voltage	Rated Dielectric Isolation Voltage
V<250 VAC	1000 VAC or 1414 VDC
V>250 VAC	1000 VAC + (2xV) VAC or 1.414 x [1000V + (2xV)] VDC
V<250 VDC	1000 VDC
V>250 VDC	1000 VDC + (2 x V) VDC

Note:
1. The rated dielectric isolation voltage must be applied for 1 minute without break down.
2. Break down is defined as a leakage current greater than 5mA, but it may be necessary to increase this limit to compensate for a significant capacitive charging current with large area IMpcb substrates.
3. The test time can be reduced to 1 second, if tested at 120% of the 1minute test voltage, but the accelerated test requires a dielectric that will withstand 120% of the rated voltage.
4. AC hipot testing is typically done at 60Hz VAC.
5. DC testing must be done at 1.414 times the specified AC rated dielectric isolation voltage.
6. These tests are based on UL508C for Power Conversion Equipment.

The IMpcb substrates or boards should be 100% hipot tested by the board fabricator, to screen-out any isolation defects, which were induced by the fabrication process.

2.2 Dielectric Strength

The Dielectric Strength of the T-preg material is nominally 1200V/mil, although when it is laminated in an IMpcb structure, the dielectric strength must be de-rated for process and thickness variations, and other manufacturing irregularities. Figure 2.1 shows the Dielectric Strength versus Dielectric Thickness of 1KA T-preg of the Single-Sided substrates or DSL boards. Multi-layer dielectric strength may be rated lower depending on number of layers, dielectric thickness, foil thickness and foil layout, and should be assessed for each product.

The ideal T-preg dielectric strength, and the rated AC and DC dielectric strength are shown below for select dielectric thickness of Single Sided substrates and DSL boards.

Dielectric Thickness (Nominal)	Dielectric Isolation Voltages VDC (Ideal)	VAC (Rated)	VDC (Rated)
0.004”	4800V	2000V	3000V
0.005”	6000V	2500V	3500V
0.006”	7200V	3000V	4200V
0.007”	8400V	3500V	5000V
0.008”	9600V	4000V	5500V
0.010”	12000V	4500V	6000V

2.3 Reliability and Operational Life

The T-preg dielectric has excellent dielectric strength, and can be superior to ceramic and FR4, if used properly. These advantages arise from the inert low loss filler, and the flexibility of the organic resin under thermo-mechanical expansion stresses. As with all organic materials, it is important to operate the materials under conditions where it remains stable, so that all thermal, physical and electrical properties are maintained. There are three important factors that can influence reliability of the IMpcb dielectric: (1) Thermal Aging, (2) AC Life and (3) DC Life.

2.3.1 Thermal Aging

The 1KA T-preg is recognized by UL for continuous operation at 130°C. The dielectric has been tested at accelerated temperatures to rate it at 130°C for 100,000 hours of operation. These tests are based on the UL1557 aging curve. The T-preg materials will also withstand multiple soldering operations at 260°C. The T-preg dielectric can be operated with peak temperatures or local temperatures above the continuous maximum temperature rating, if the application voltages are sufficiently benign.

2.3.2 AC Life

The AC hipot testing only assures that there are no dielectric defects, and that the dielectric does not breakdown, which is sufficient to insure isolation in most applications. In high voltage AC applications, it is possible to have micro arcing within the dielectric, which can cause dielectric breakdown over time. If such arcing exists, the wear-out or aging will be accelerated with higher voltage and higher frequency.

The aging mechanism can be eliminated by selecting a dielectric type and thickness that will not allow micro arcing under the worst case operating conditions. The micro arcing is called Partial Discharge, and the minimum voltage that micro arcing begins is called the “Corona Inception Level”(CIL). Micro arcing is typically defined as a discharge of greater than 5 pC per cycle, which is also the VDE criteria for CIL. There is a corresponding level, which the voltage must be reduced to for the partial discharge to stop, and that voltage is called the “Corona Extinction Level”(CEL).

The Maximum AC Voltage versus Dielectric Thickness for the 1KA T-preg is shown in Figure 2.2a, and should be considered as the V(peak) or V(max) of the product application. In applications where there are frequent transient voltages in excess of the CIL rating, the CEL may need to be specified. See VDE test procedures and conditions for the recommended partial discharge testing details.

It is recommended that for high voltage AC application, the dielectric thickness selected be based on all three (3) parameters shown in Figure 2.2a: a) Continuous nominal Vrms, b) Peak Recurring voltage, and c) Corona Inception Level. These voltages are shown below for select dielectric thickness:

Dielectric Thickness (Nominal)	Vrms Continuous (Nominal)	Vpeak Recurring (Maximum)	Corona Inception (Nominal)
0.004”	200V	500V	1200V
0.005”	250V	625V	1500V
0.006”	400V	1000V	2000V
0.007”	500V	1250V	2500V
0.008”	550V	1350V	3000V
0.010”	650V	1625V	3300V

2.3.3 DC Life

High voltage DC applications may add additional constraints to the selection of dielectric type and thickness. High DC voltages can produce failures in time, because of ionic impurities. Wear-out may be accelerated with temperature, humidity and high DC voltage. Therefore, it is important to choose the appropriate material and thickness for high voltage applications. If the IMpcb is operated above the glass transition temperature (Tg), contaminants can become mobile at high voltages. In continuous high voltage DC applications, it is important to select a dielectric thickness that will not have DC wear-out at the maximum substrate operating temperature.

The maximum recommended continuous DC operation voltages for 1KA T-preg, are shown in Figure 2.2b as a function of dielectric thickness, and for operation below the Tg and above the Tg. The recommended maximum continuous DC voltages at select dielectric thickness are shown below:

Dielectric Thickness (Nominal)	VDC @ Temp.<Tg (Maximum)	VDC @ Temp.>Tg (Maximum)
0.004”	480V	320V
0.005”	600V	400V
0.006”	720V	480V
0.007”	840V	560V
0.008”	960V	640V
0.010”	1100V	750V

The 1KA T-preg materials have been tested at 120% of the maximum rated continuous DC voltage for 1000 hours at the 1008C and 1258C, for select standard thicknesses. The glass transition temperature of 1KA T-preg is 105 to 1108C. In severe applications, it is recommended that specific products be qualified at 120% of actual maximum continuous VDC and at the maximum operating temperature.

3.0 Foil Resistivity

The copper foil used for the IMpcb is identical to foil used on standard FR4 PCB, although generally thicker, because the IMpcb is often used for higher power products. The better thermal properties of the IMpcb keep the tracks cooler, which reduces the resistivity, for a given current level. The bulk resistivity of copper is 0.67 micro-ohms @ 208C and 0.96 micro-ohms @ 1308C.

The sheet resistivity for 1 oz through 4 oz copper are given in Figure 3.1, at 208C and 1308C, and the sheet resistivity of selected copper foil weights are shown below at 20 and 1308C. The relationship between sheet resistivity and track resistance is given below, as a function of line length, width and thickness.

Copper Foil Wt.	Sheet Resistivity (milli-ohms/square) @ 208C	@ 1308C
1oz	0.48	0.69
2oz	0.24	0.34
3oz	0.16	0.23
4oz	0.12	0.17

R = rL/W, where
R = Resistance (milli-ohms)
r = Sheet Resistivity (milli-ohms/square)
L = Length of Track (inch)
W = Width of Track (inch)

4.0 Maximum Copper Foil Current

The maximum track current carrying capability for the IMpcb is significantly higher than that of a standard FR4 PCB. The primary reason is that the higher thermally conductive T-preg dielectric takes the heat away, and the secondary effect is the lower resistivity at the lower operating temperature, based on the TCR of copper.

The maximum currents are based on a ΔT of 50C8 and a maximum foil temperature of 1308C, and are shown in Figure 4.1a through 4.1f, which provides Maximum Current versus Line Width. The six (6) Figures represent dielectric thickness of 0.004", 0.006", 0.008", 0.010", 0.012" and 0.020" , and all show lines for 1oz, 2oz, 3oz and 4oz copper.

Incremental maximum currents with design guard-bands are shown below for select dielectric thicknesses:

Foil Wt.	Line Width	Dielectric Thickness (inches) 0.004	0.006	0.008	0.010	0.012	0.020
1oz	0.010"	9A	8A	7A	6A	5A	4A
1oz	0.020"	19A	15A	13A	12A	11A	11A
1oz	0.050"	47A	38A	33A	30A	27A	21A
1oz	0.100"	94A	77A	67A	60A	54A	42A
1oz	0.250"	235A	192A	166A	149A	136A	105A
2oz	0.010"	13A	11A	9A	8A	8A	6A
2oz	0.020"	27A	22A	19A	17A	15A	12A
2oz	0.050"	67A	54A	47A	42A	38A	30A
2oz	0.100"	133A	109A	94A	84A	77A	60A
2oz	0.250"	333A	272A	235A	211A	192A	149A
3oz	0.010"	16A	13A	12A	10A	9A	7A
3oz	0.020"	33A	27A	23A	21A	19A	15A
3oz	0.050"	82A	67A	58A	52A	47A	36A
3oz	0.100"	163A	133A	115A	103A	94A	73A
3oz	0.250"	408A	333A	288A	258A	235A	182A
4oz	0.010"	19A	15A	13A	12A	11A	8A
4oz	0.020"	38A	31A	27A	24A	22A	17A
4oz	0.050"	94A	77A	67A	60A	54A	42A
4oz	0.100"	188A	154A	133A	119A	109A	84A
4oz	0.250"	471A	384A	333A	298A	272A	211A

Notes: 1. These are recommended design currents, which are guard-banded at 80% of the calculated maximum currents. The guard-band is intended to compensate for tolerances in dimensions and material properties.
2. If you need data maximum currents at different conditions, please contact Thermagon for application support.

5.0 Capacitance

The T-preg dielectric has a unique filler system, with a low dielectric constant and low dielectric loss, relative to competitive thermal materials. The dielectric constant is 4.33 @ 1KHz 4.09 @ 1 MHz. The capacitance per square inch versus dielectric thickness is shown in figure 5.1. This low capacitance reduces capacitive coupling, and associated noise, cross talk and ground current. These advantages may be even more important at higher frequencies and higher voltages. The associated low dielectric loss is also important in many applications.

The capacitance per square inch for incremental thickness is shown below:

Dielectric Thickness	Capacitance @ 1 KHz		Capacitance @ 1 MHz	
(inches)	(pF/sq.in.)	(pF/sq.cm.)	(pF/sq.in.)	(pF/sq.cm.)
0.004	244	38	230	36
0.006	162	25	153	24
0.008	122	20	115	18
0.010	97	15	92	14
0.012	81	13	77	12
0.020	49	8	46	7

C = 0.225KA/t, where C = Capacitance (pF)
K = Dielectric Constant
A = Pad Area (square inches)
t = Dielectric Thickness (inch)

The capacitance per area is based on an infinite plane. When it is important to calculate the actual capacitance value, use actual area plus an additional edge effect. The edge effect can be simulated by adding 1.2 times the dielectric thickness to the perimeter of the pad or track.

6.0 Inductance

The IMpcb offers an extremely low track inductance, relative to wires, standard PCB tracks, ceramic substrate tracks, connector, and terminals. The thin dielectric layer between the tracks and the base plate provides inductance reduction, similar to a laminated bus bar with an equal current in the opposite direction. This allows devices to be switched at higher di/dt's with lower peak switching voltages and with lower switching losses. The lower switching voltage peaks may allow the use of lower voltages switching devices, which can inherently reduce device cost and conduction losses.

The precise inductance calculation can be quite complex for specific layout geometries, but it is possible to make some good estimates under special conditions. Because inductance is important to applications at high frequencies or high di/dts, it is possible to consider only the external inductance, or to say that L = L(ext) at high frequencies greater than 1 Mhz or at high di/dts greater than 1000A/uS.

L = L(ext) = 32.0 t L/W, where L = Inductance at f > 1 MHz (nH)
L(ext) = External Inductance (nH)
T = Dielectric Thickness (inches)
L = Track Length (inches)

W = Track width (inches)

Since, low inductance is most important at high frequencies or high di/dts, this equation is sufficient for estimating noise or peak voltages, in such applications. A very rough rule of thumb for the inductance at 1 KHz is 3.6 times the L(ext). Figure 6.1 shows the Inductance per inch versus Line Width, for IMpcb tracks at 1 MHz and for 4-20 mil dielectric thickness and for 10-250 mil line width. The following table provides the IMpcb track Inductance @ 1 MHz for some selected dielectric thicknesses and line widths.

Dielectric Thickness (inches)	Inductance per Inch of Track (nH) for Line Widths of 10mil	25mil	50mil	100mil	250mil
0.004	12.8	5.1	2.6	1.3	0.5
0.006	19.2	7.7	3.8	1.9	0.8
0.008	25.6	10.2	5.1	2.6	1.0
0.010	32.0	12.8	6.4	3.2	1.3
0.012	38.4	15.4	7.7	3.8	1.5
0.020	64.0	25.6	12.8	6.4	2.6

This is Effective Inductance at high frequency or high di/dt, and it will allow the calculation of voltage spikes resulting from high di/dts.

$\Delta V = L\ di/dt$, where ΔV = Induced Voltage Spike (volts)
L = Effective Inductance @ high frequency (H)
di/dt = Rate of Current Change (A/sec)

For example, if you switch a device at a di/dt = 1500A/uS, and you have a stray inductance of 5 nH, the resulting voltage spike will be 7.5 volts. In most products, associated devices, terminals and connectors make a much larger contribution to the stray inductance than long IMpcb tracks.

7.0 Electrical Vias between Foil Layers

As with standard printed circuit boards, copper plated vias are used to make electrical connections through the T-preg dielectric layers, connecting tracks on different foil layers. In a standard PCB, the FR4 acts as a thermal insulator, and the via current ratings are limited by the FR4 thermal conductivity and associated allowable temperature rise.

7.1 Maximum Via Current

The IMpcb Vias have a much higher current rating, because the T-preg dielectric provides excellent thermal conduction of the heat from the vias, and because the metal base plate removes or distributes the heat generated by the vias.

The maximum via currents have been calculated for an IMpcb with two layers of copper foil, and two T-preg dielectric layers, all on an aluminum base plate. The vias are between the copper foil layers. The maximum base plate temperature has been set at 80°C, and the current required to raise the Via to a temperature of 130°C has been calculated. Figure 7.1a-d shows the Maximum Via Current versus Dielectric Thickness with 13, 21 and 30 mil vias, and with 50 and 100 mil via pitch or center-to-center spacing.

The maximum via currents are calculated with hexagonal pad of copper foil in both foil layers. The pads and vias form a thermal cell, with an area of 0.864 times the via pitch. The maximum via currents apply to an individual cell, or an array of cells. The vias also enhances the thermal conductivity from a pad on the upper foil to the base plate, and the thermal resistance of the Thermal Via Pads are presented in section 8.0.

The Maximum Via Currents with 50 mil pitch, ΔT=50ºC and 2 oz Cu foils with 1 mil Cu plating are shown below with 13, 21 and 30 mil vias, and for dielectric layers of 0.006", 0.008", 0.010" and 0.012".

Via Diameter (inches)	Lower Dielectric Thickness (inches)	Upper Dielectric Thickness (inches)	Maximum Calculated Via Current (amperes)	Maximum Via Current with Guard-band (amperes)
0.013	0.006	0.006	83	62
0.013	0.008	0.008	63	47
0.013	0.010	0.010	50	38
0.013	0.012	0.012	42	33
0.021	0.006	0.006	107	80
0.021	0.008	0.008	80	60
0.021	0.010	0.010	65	49
0.021	0.012	0.012	54	41
0.030	0.006	0.006	120	90
0.030	0.008	0.008	90	68
0.030	0.010	0.010	72	54
0.030	0.012	0.012	60	45

These maximum currents shown are calculated based on the maximum rated temperature, and the actual designs should be guard-banded to accommodate material, process and design variations and tolerances. As with other parameters, the necessary guard-band will vary with product and application, but it is typical to design for 75% of the calculated maximum current.

7.2 Maximum Via Resistance

The via may be the thinnest copper interconnect on the IMpcb layout. At the maximum current, the via temperature may be as high as 130ºC. At 130ºC the resistivity of copper is 0.94 uohm-inch, and the via resistance has been calculated based on 130ºC. The Maximum Via Resistance versus Dielectric thickness is shown in Figure 7.2a and 7.2b for a number of via sizes and plating thicknesses. The via resistance at nominal currents will be less than at maximum current, and can be calculated based on the TCR of the copper and the actual via temperature. Single Via resistances with 50 mil pitch, ΔT=50ºC and 2 oz Cu foils with 1 mil Cu plating are shown below with 13, 21 and 30 mil vias, and for dielectric layers of 0.006", 0.008", 0.010" and 0.012".

Via Diameter (inches)	Lower Dielectric Thickness (inches)	Upper Dielectric Thickness (inches)	Via Resistance @ 20ºC (ohms)	Via Resistance @ 130ºC or Max. Current (ohms)
0.013	0.006	0.006	1.05E-04	1.50E-04
0.013	0.008	0.008	1.40E-04	2.00E-04
0.013	0.010	0.010	1.74E-04	2.49E-04
0.013	0.012	0.012	2.09E-04	2.99E-04
0.021	0.006	0.006	0.63E-04	0.90E-04
0.021	0.008	0.008	0.84E-04	1.20E-04
0.021	0.010	0.010	1.05E-04	1.50E-04
0.021	0.012	0.012	1.26E-04	1.80E-04
0.030	0.006	0.006	0.43E-04	0.62E-04
0.030	0.008	0.008	0.58E-04	0.83E-04

0.030	0.010	0.010	0.72E-04	1.03E-04
0.030	0.012	0.012	0.87E-04	1.24E-04

These Via Resistances are guidelines, and your layout or application may vary. Therefore, it is recommended that the maximum via resistances be confirmed with FEA and/or actual measurement, on the actual design.

8.0 Thermal Vias Application

The vias between copper foil layers can significantly enhance thermal conductivity between layers. Thermal vias are much more effective in IMpcb than in standard PCBs, because IMpcb provides a means to transfer the heat from the lower layer to a heat sink, bracket or ambient. The improved thermal dissipation not only cools the vias and tracks, but also can significantly reduce the thermal resistance for power devices on the upper foil. The technique is useful in removing heat from both packaged devices and chips, and is especially effective in complex many layer board applications, like single board computers.

8.1 Thermal Resistance of Via Pads

The Thermal Resistance per Square Inch from Upper Foil to Base Plate versus Dielectric Thickness is given in Figures 8.1a-d. The graphs provide thermal conductivity for ΔT=50°C with a maximum base plate temperature of 80°C, and for 13 mil, 21 mil & 30 mil vias, and for 50 & 100 mil via pitch. The dielectric thicknesses shown are per layer, and include the range from 0.006" to 0.012".

As with the electrical vias, these thermal resistance values between upper foil and base plate, are based on a hexagonal cell of metal in both foil layers. Extending the inner foil layer or increasing copper thickness can reduce the thermal resistance further. Typically, these reductions will be small, but in some layouts and applications, they can offer significant improvements.

8.1.2 The Thermal Resistance per square Inch is shown below for selected dielectric thicknesses, selected via size, ΔT=50°C, T(base)=80°C, 2 oz Cu foil with 1 mil Cu plating, and a 50 mil via pitch.

Via Diameter (inches)	Lower Dielectric Thickness (inches)	Upper Dielectric Thickness (inches)	Thermal Resistance per Square Inch (°C/W)	Thermal Resistance per Square Inch with Guard-band (°C/W)
0.013	0.006	0.006	0.105	0.126
0.013	0.008	0.008	0.137	0.164
0.013	0.010	0.010	0.170	0.204
0.013	0.012	0.012	0.203	0.244
0.021	0.006	0.006	0.106	0.127
0.021	0.008	0.008	0.140	0.168
0.021	0.010	0.010	0.173	0.208
0.021	0.012	0.012	0.207	0.248
0.030	0.006	0.006	0.121	0.145
0.030	0.008	0.008	0.160	0.192
0.030	0.010	0.010	0.199	0.239
0.030	0.012	0.012	0.239	0.287

8.1.3 The Thermal Resistance per square Inch is shown below for selected dielectric thicknesses: selected via size, ΔT=50C8, T(base)=808C, 2 oz Cu foil with 1 mil Cu plating, and a 100 mil via pitch.

Via Diameter (inches)	Lower Dielectric Thickness (inches)	Upper Dielectric Thickness (inches)	Thermal Resistance per Square Inch (C8/W)	Thermal Resistance per Square Inch with Guard-band (C8/W)
0.013	0.006	0.006	0.156	0.187
0.013	0.008	0.008	0.199	0.239
0.013	0.010	0.010	0.243	0.292
0.013	0.012	0.012	0.286	0.343
0.021	0.006	0.006	0.138	0.166
0.021	0.008	0.008	0.177	0.212
0.021	0.010	0.010	0.215	0.258
0.021	0.012	0.012	0.253	0.304
0.030	0.006	0.006	0.130	0.156
0.030	0.008	0.008	0.167	0.200
0.030	0.010	0.010	0.203	0.244
0.030	0.012	0.012	0.240	0.288

8.2 General Thermal Via Considerations:

As with the electrical via, a design guard-band is recommended to accommodate process, material and layout variations and tolerances. Typically a 20% guard-band will be sufficient, but this may vary with product and application. Therefore, the necessary guard-band should be determined by FEA and/or testing, for critical applications.

Thinner dielectric layers can best reduce the thermal resistance, and a thinner lower dielectric layer will provide the best improvement to thermal via configurations. More small vias will typically reduce the thermal resistance, but will add cost. Thicker copper will also reduce thermal resistance, but at increased cost for both materials and manufacturability. For example, with 0.006” dielectrics, 13 mil vias, 50 mil pitch and 50C8 delta T, the thermal resistance per square inch is; 0.083 C8/W with 1 oz copper plus 1.0 mil Cu plating, and 0.077 C8/W with 2 oz copper with 1.4 mil Cu plating.

8.3 Thermal Vias in Applications without Base Plates

Thermal Vias can provide significant thermal improvement in products without a base plate. Copper foils can be used as thermal planes to distribute heat over the entire available board surface, and heat can be transferred to the thermal planes through vias and/or isolated adjacent pads. Heat dissipation can be optimized by uniformly distributing the heat across the board, which can be done with component placement and thicker thermal copper planes. Once the board is at a relatively uniform temperature, more copper will add only cost. Also, once the board is at a common temperature, the thermal resistance from board to ambient can more be easily estimated.

These techniques are useful when heat sinks are not available, and they can be enhanced with forced air or thermal mounting brackets to the thermal plane. The T-preg dielectric is relatively soft and flexible, and may require additional support when not used with a base plate. This is often done by including a thin layer of FR4 in the lamination. This may be required for large boards, heavy components, or for boards that serve a structural function. The FR-4 may also be required in an unbalanced layout that would warp from thermo-mechanical stresses. The thickness and location of support boards should be chosen to not limit the thermal performance of the system.

Figure 1.1a: 1KA Thermal Resistance per Square Inch

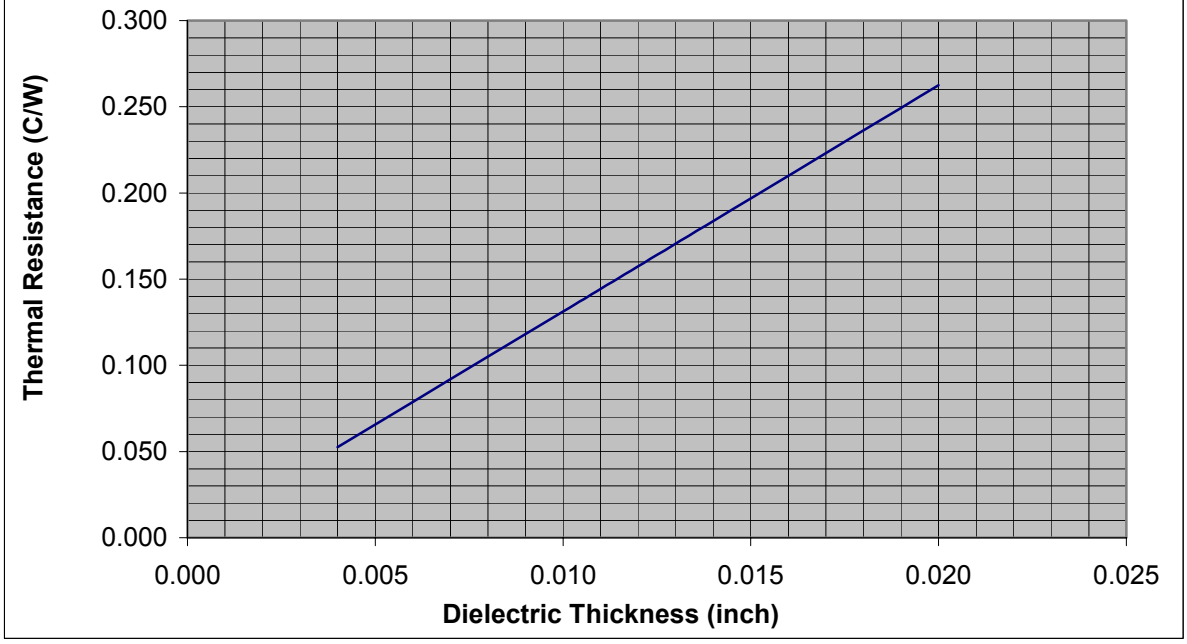

Figure 1.1b: 1KA Thermal Resistance per Square Centimeter

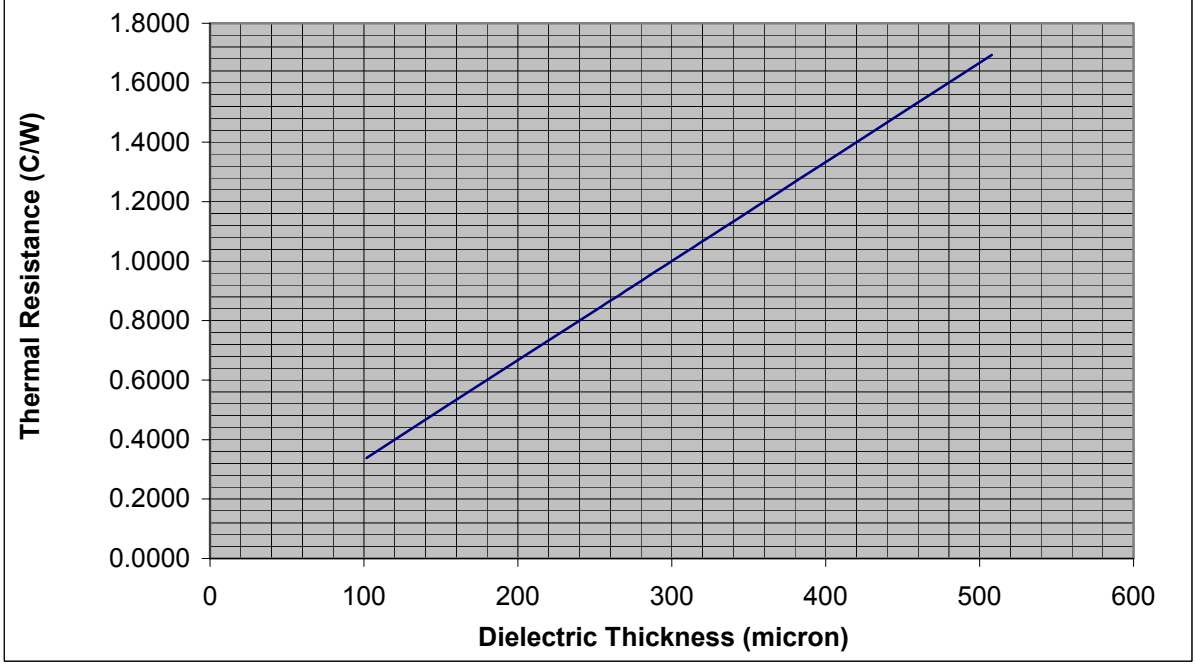

Figure 1.2: Thermal Resistance vs 1KA Dielectric Thickness of IMpcb Pads with 2 oz Cu and 0.062" Al Base

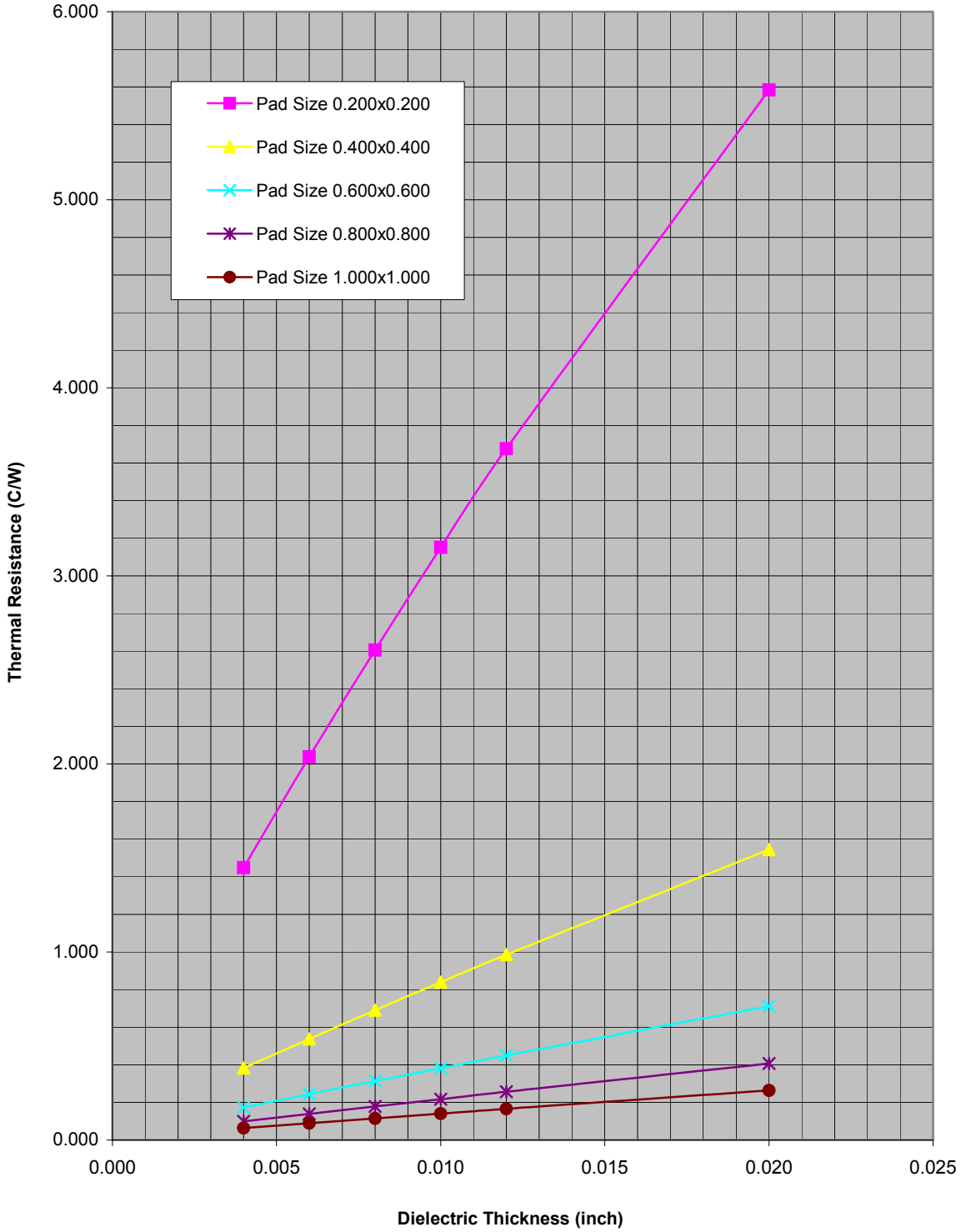

Figure 2.1: Dielectric Strength vs Dielectric Thickness

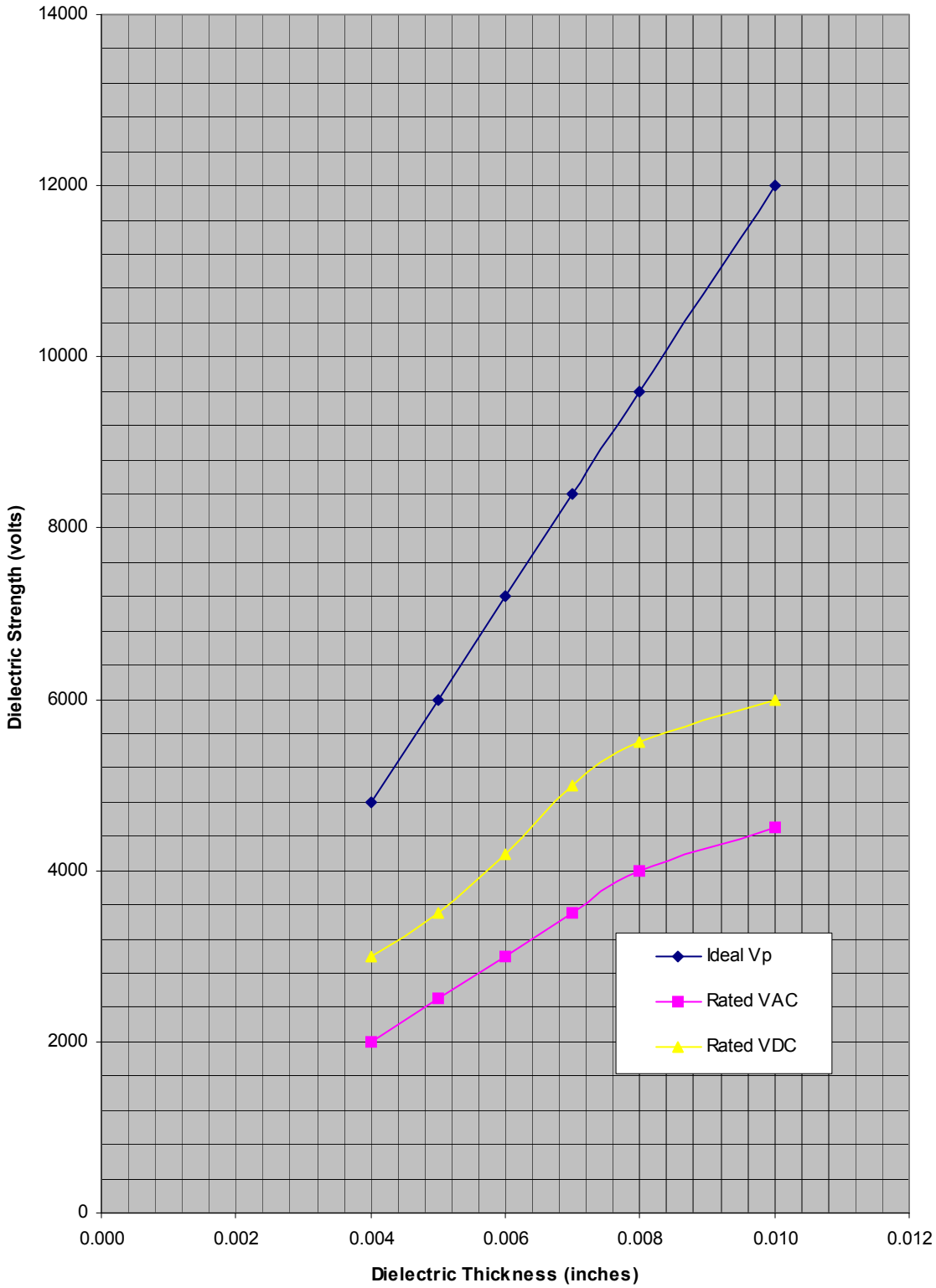

Figure 2.2a: Maximum AC Voltage vs Dielectric Thickness

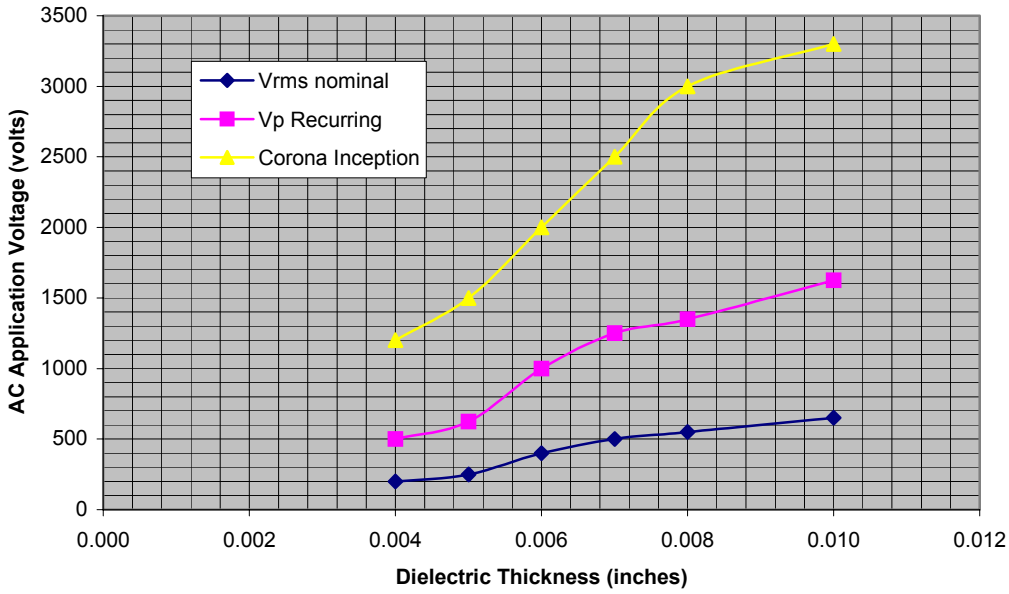

Figure 2.2b: Maximum DC Continuous Voltage vs Dielectric Thickness

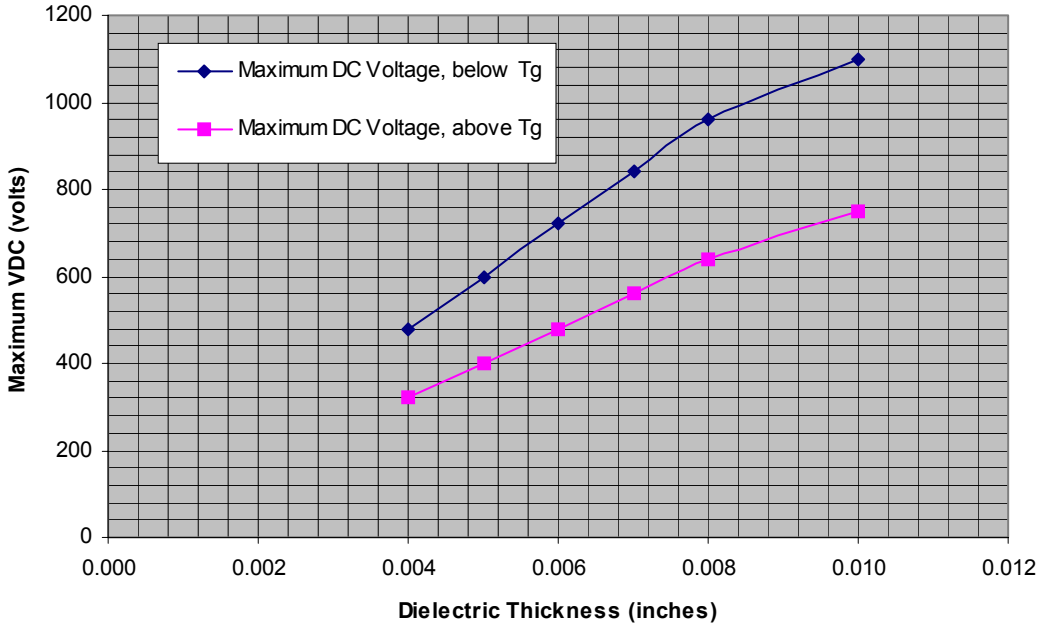

Figure 3.1: Copper Foil Sheet Resistivity vs Foil Weight

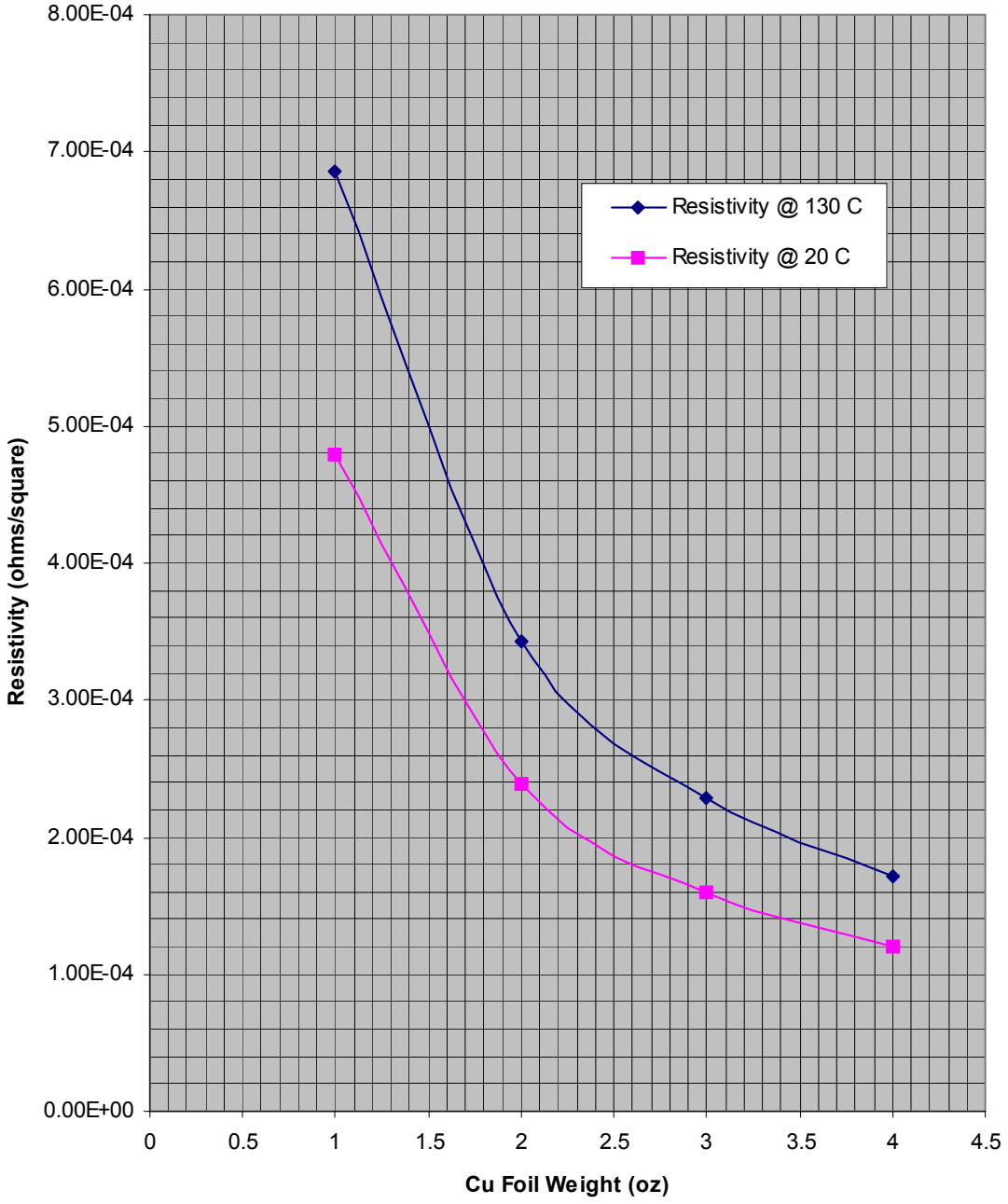

Figure 4.1a: Max. Steady-State Current vs Line Width
@ 0.004" 1KA Dielectric & delta T = 50 C

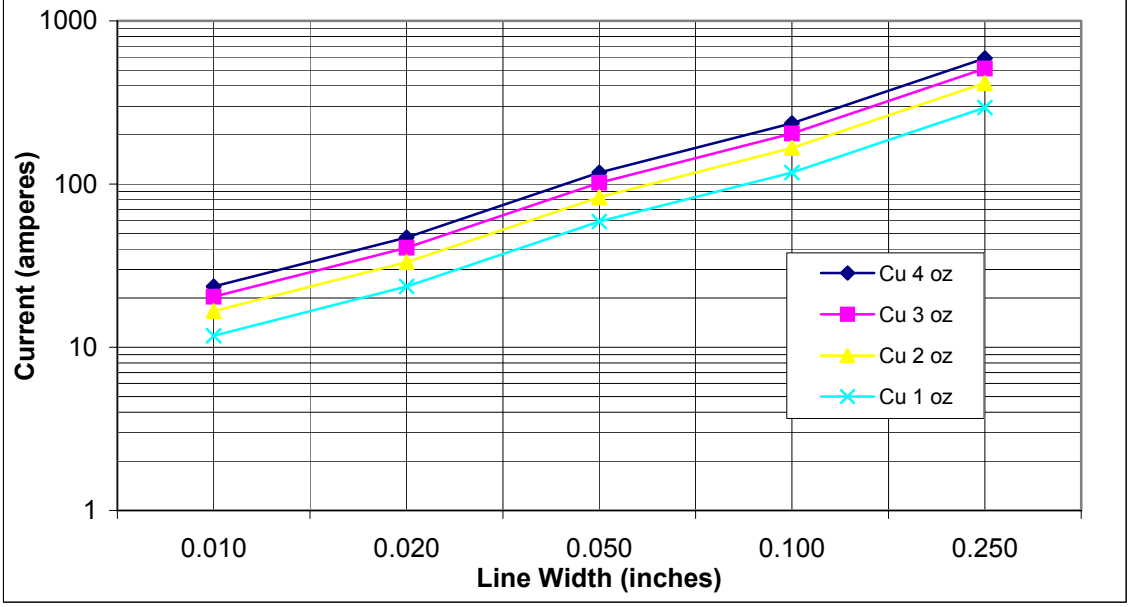

Figure 4.1b: Max. Steady-State Current vs Line Width
@ 0.006" 1KA Dielectric & delta T = 50 C

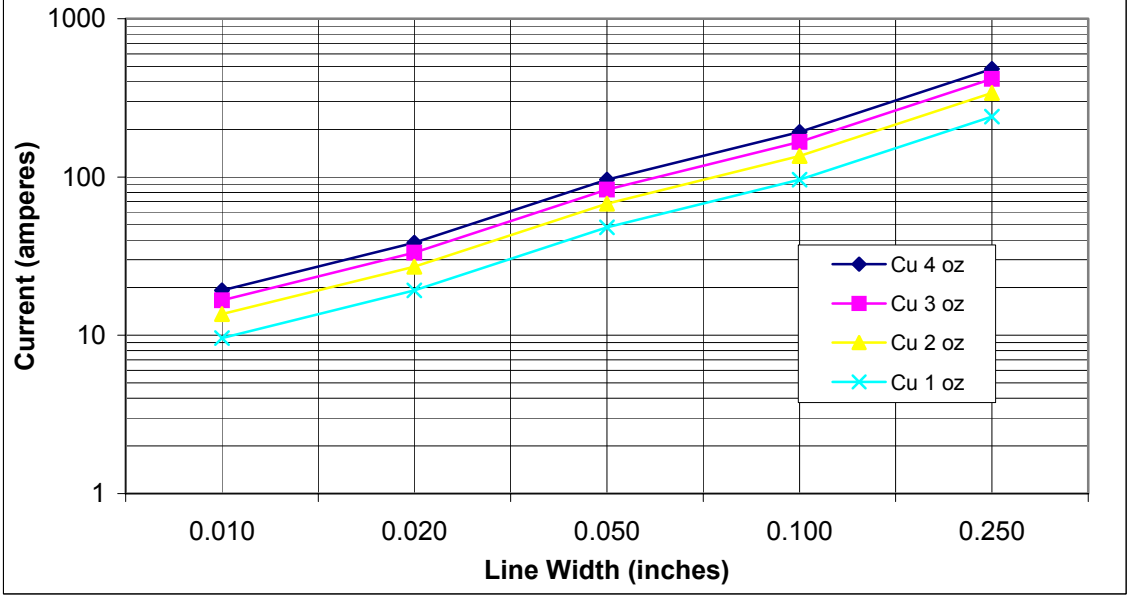

Figure 4.1c: Max. Steady-State Current vs Line Width @ 0.008" 1KA Dielectric & delta T = 50 C

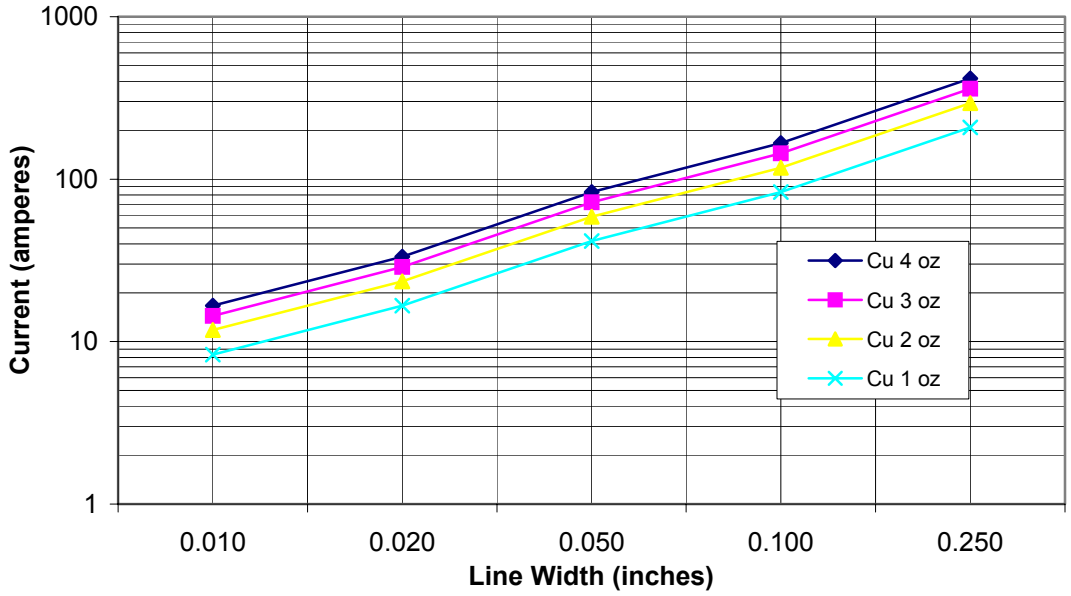

Figure 4.1d: Max. Steady-State Current vs Line Width @ 0.010" 1KA Dielectric & delta T = 50 C

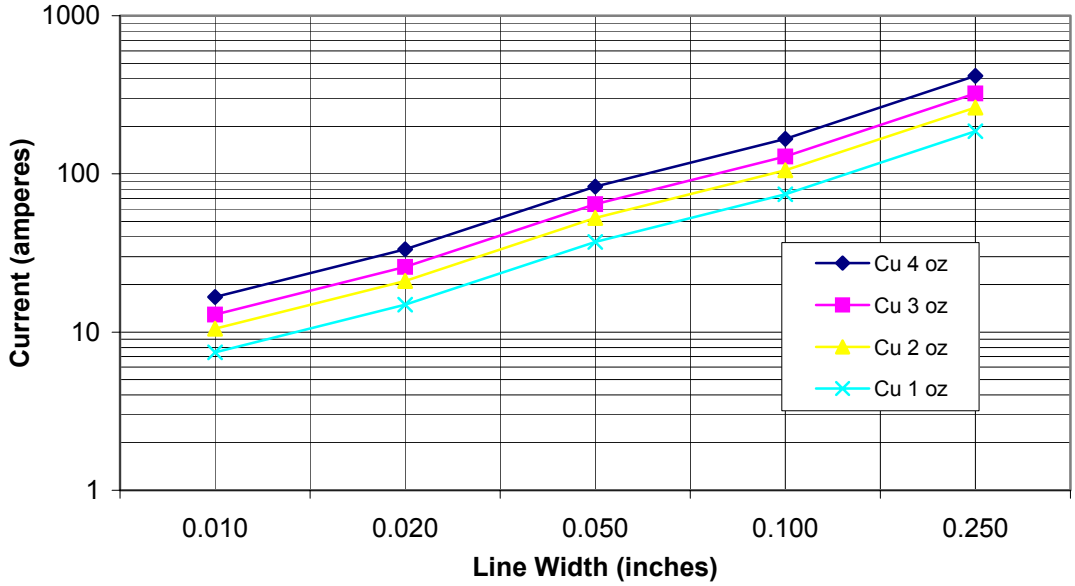

Figure 4.1e: Max. Steady-State Current vs Line Width
@ 0.012" 1KA Dielectric & delta T = 50 C

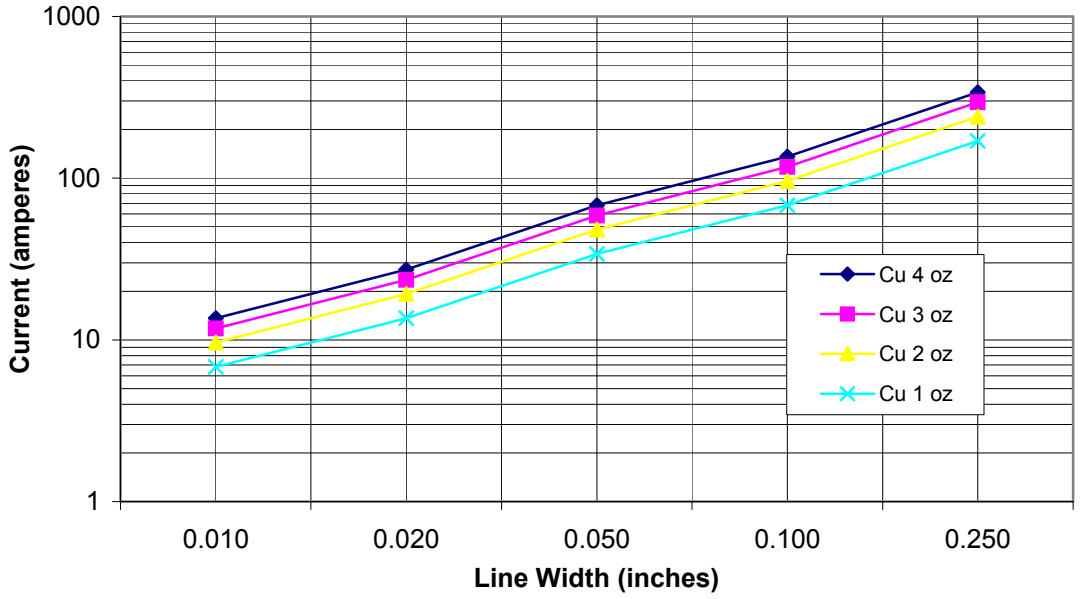

Figure 4.1f: Max. Steady-State Current vs Line Width
@ 0.020" 1KA Dielectric & delta T = 50 C

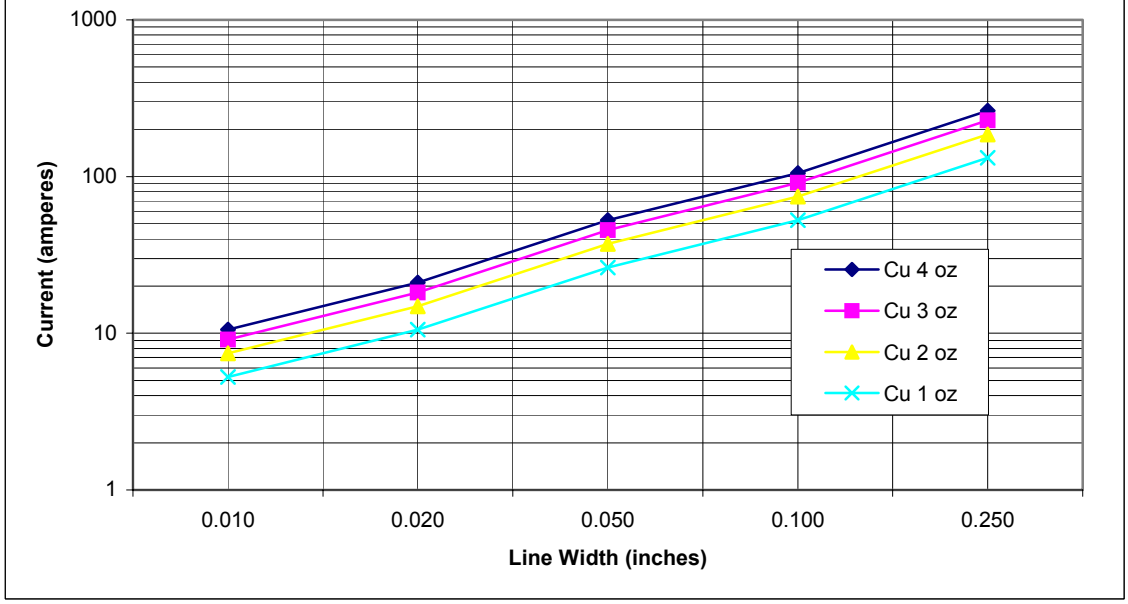

Figure 5.1: 1KA Capacitance vs Dielectric Thickness

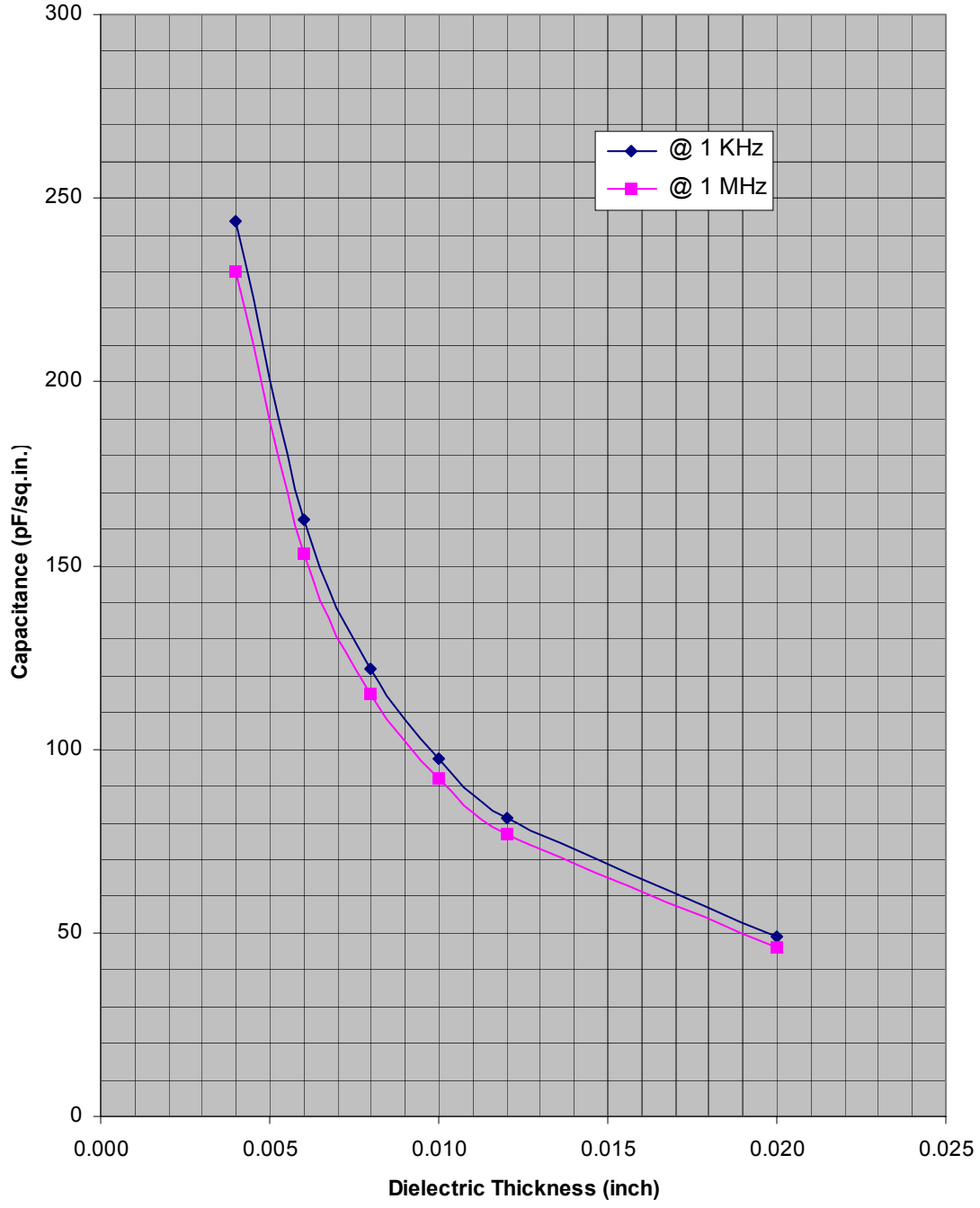

Figure 6.1: Inductance vs Dielectric Thickness, for 10-250 mil Lines @ f>1 MHz or di/dt>1000A/uS

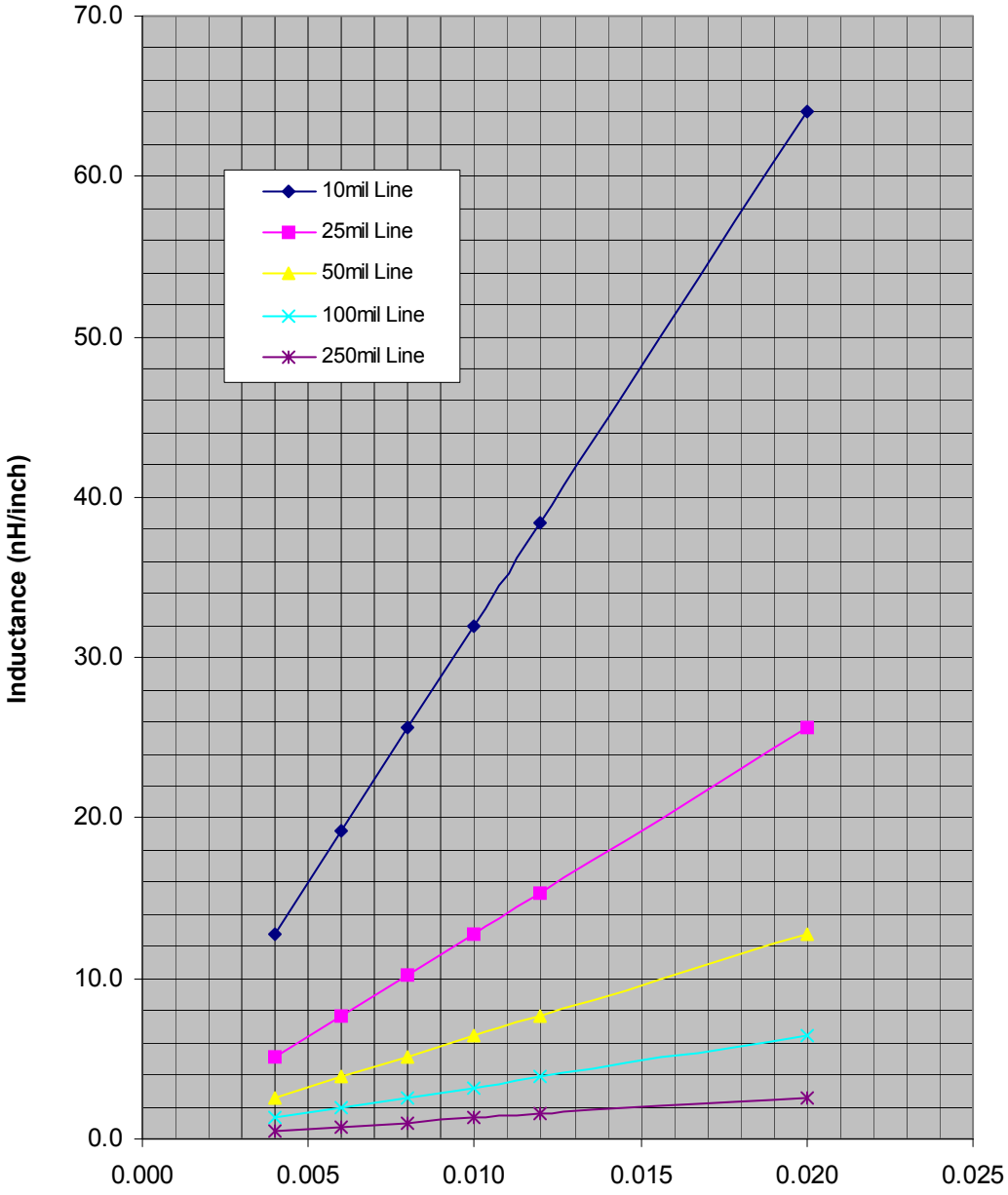

Figure 7.1a: Max. Via Current vs 1KA Dielectric Thickness for 50mil Pitch, 2 oz foil with 1mil plating & delta T=50 C

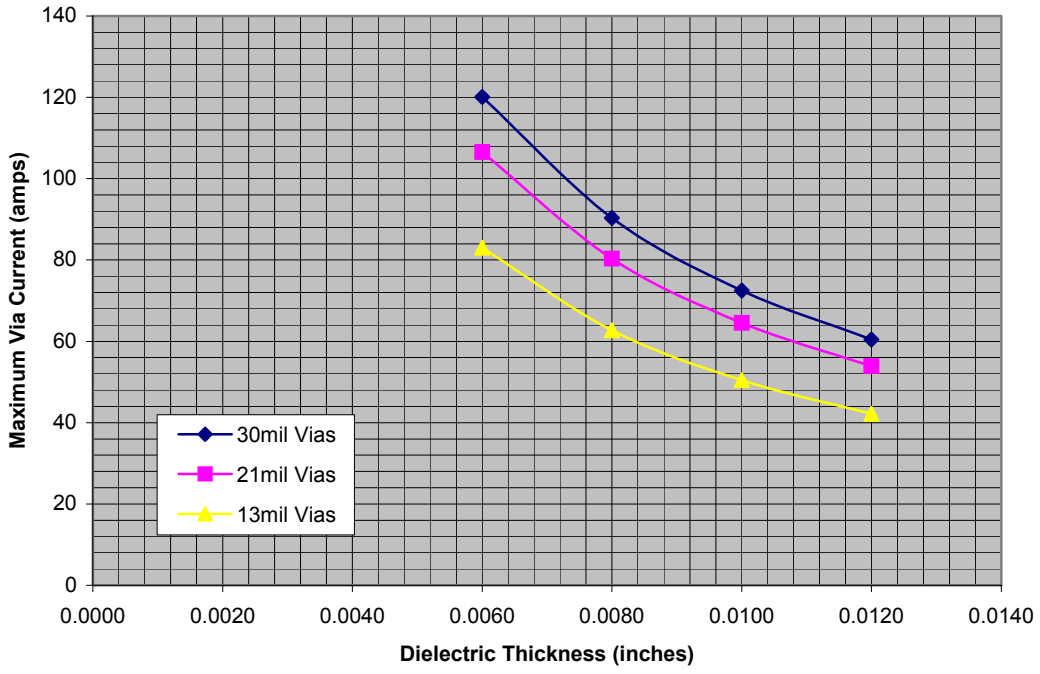

Figure 7.1b: Max. Via Current vs 1KA Dielectric Thickness for 50mil Pitch, 2 oz foil with 1.4mil plating & delta T=50 C

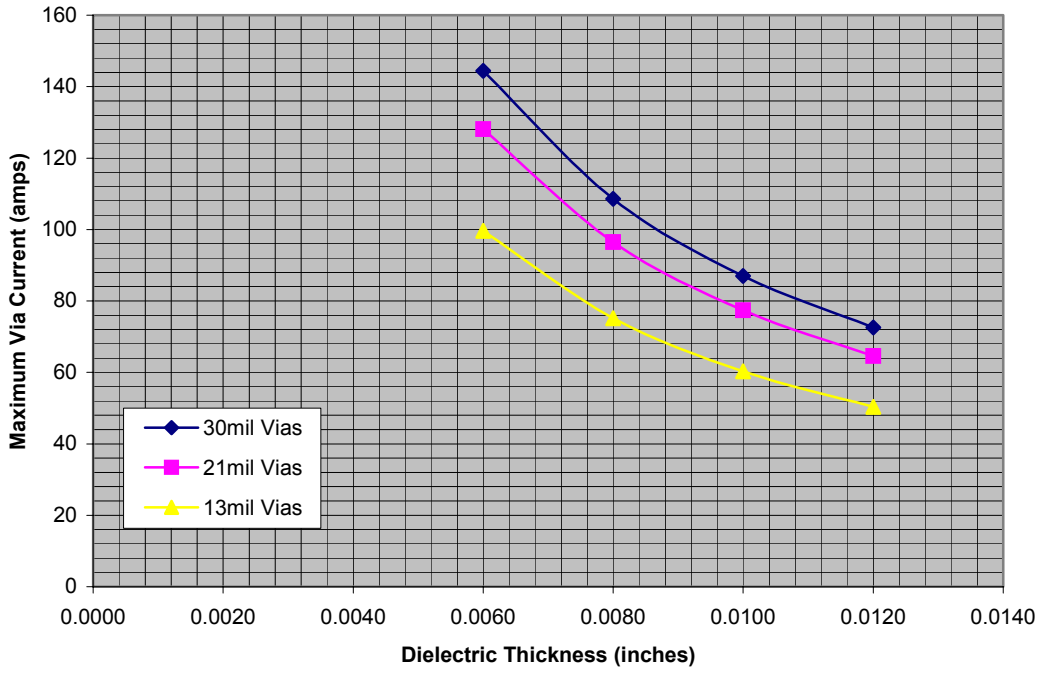

Figure 7.1c: Max. Via Current vs 1KA Dielectric Thickness for 100mil Pitch, 2 oz foil with 1mil plating & delta T=50 C

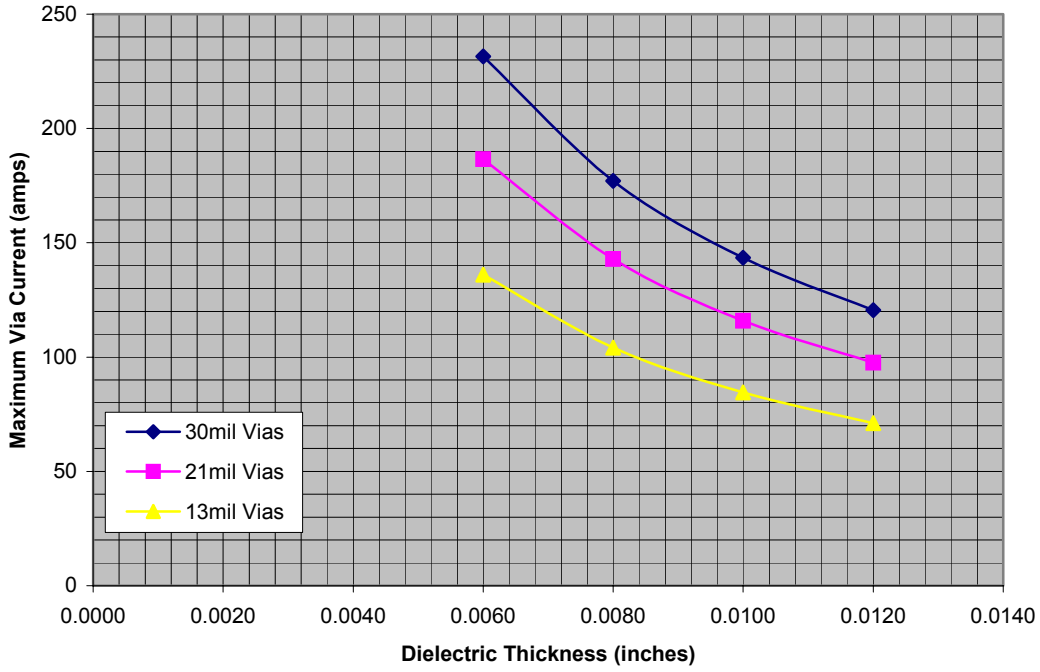

Figure 7.1d: Max. Via Current vs 1KA Dielectric Thickness for 100mil Pitch, 2 oz foil with 1.4mil plating & delta T=50 C

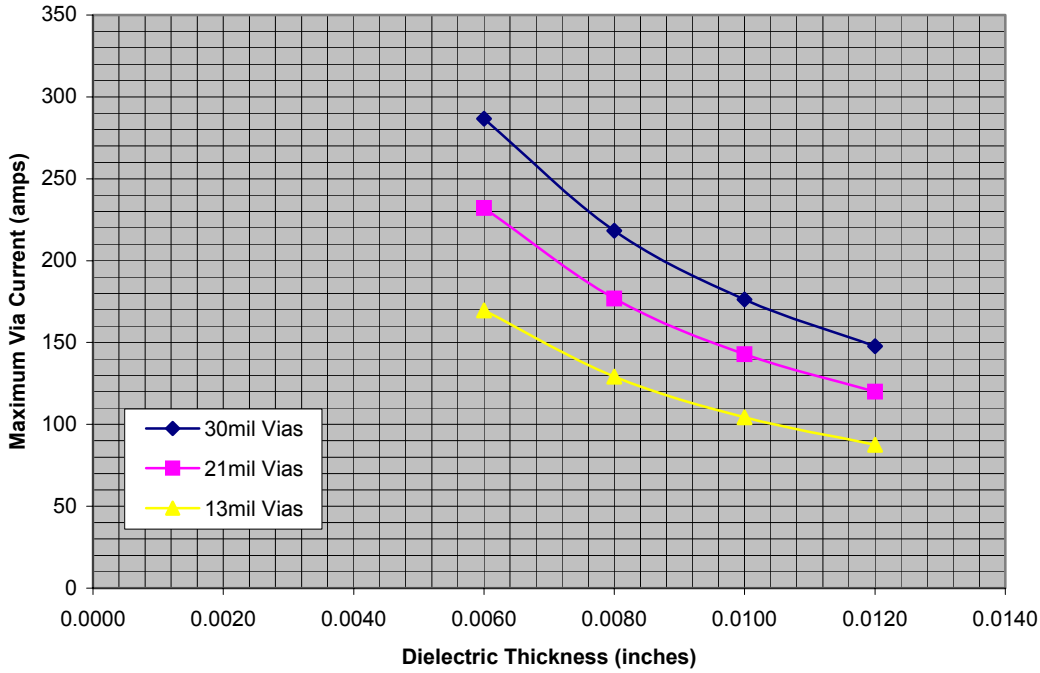

Figure 7.2a: Via Resistance vs Dielectric Thickness for 1 mil Plating and at Maximum Current

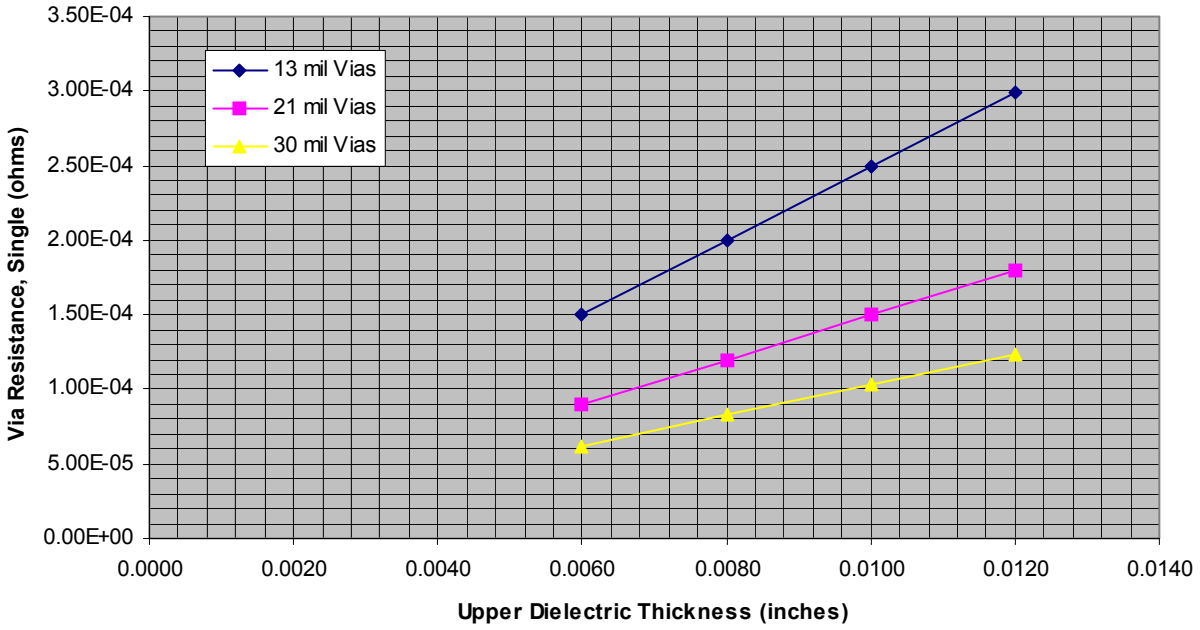

Figure 7.2b: Via Resistance vs Dielectric Thickness for 1 mil Plating and at Maximum Current

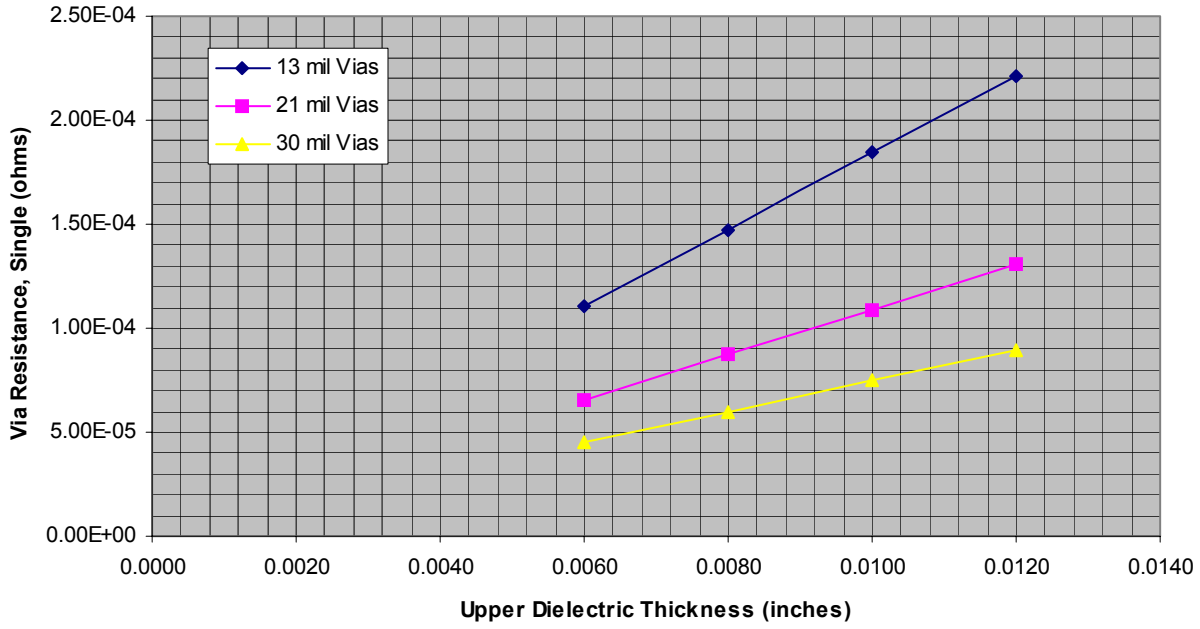

Figure 8.1a: Thermal Resistance vs 1KA Dielectric Thickness for 50mil Pitch, 2 oz foil with 1mil plating & delta T=50 C

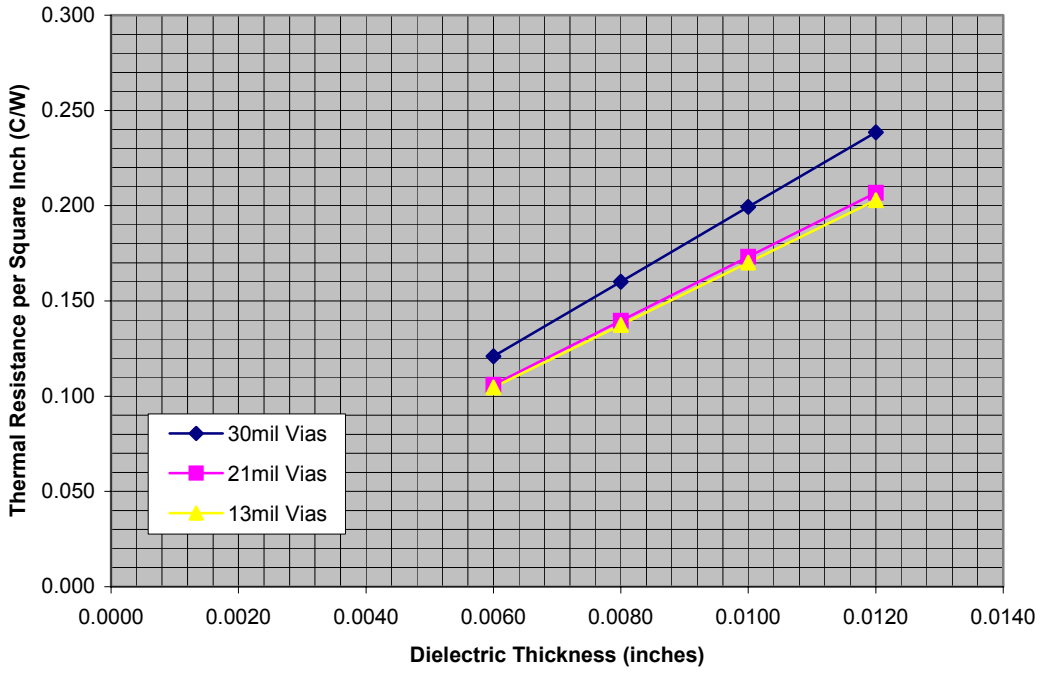

Figure 8.1b: Thermal Resistance vs 1KA Dielectric Thickness for 50mil Pitch, 2 oz foil with 1.4mil plating & delta T=50 C

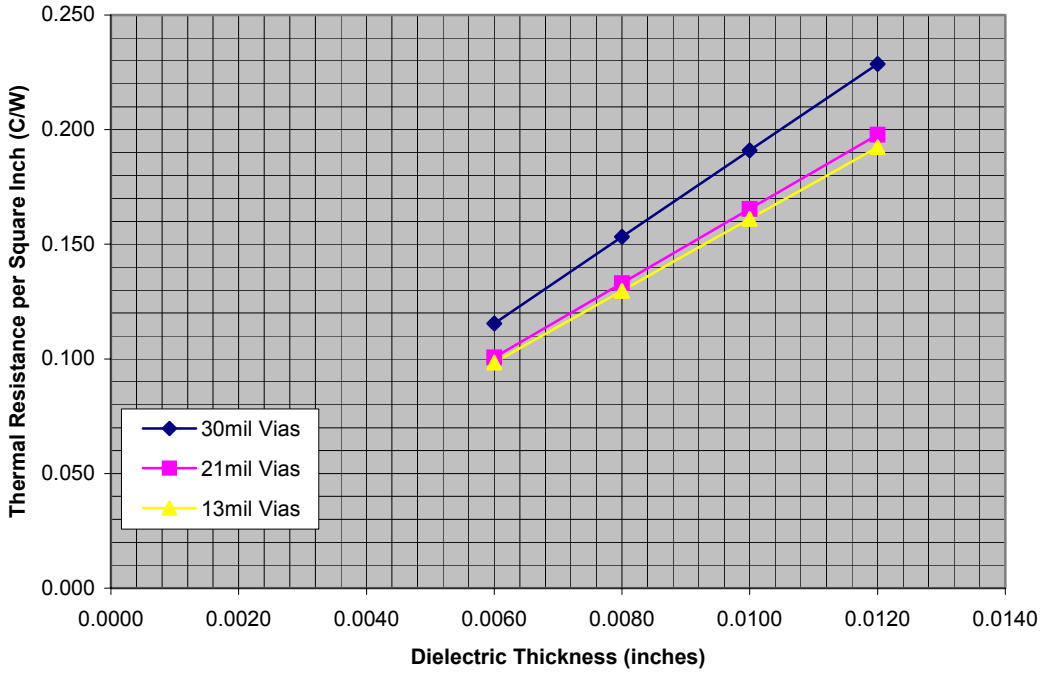

Figure 8.1c: Thermal Resistance vs 1KA Dielectric Thickness for 100mil Pitch, 2 oz foil with 1mil plating & delta T=50 C

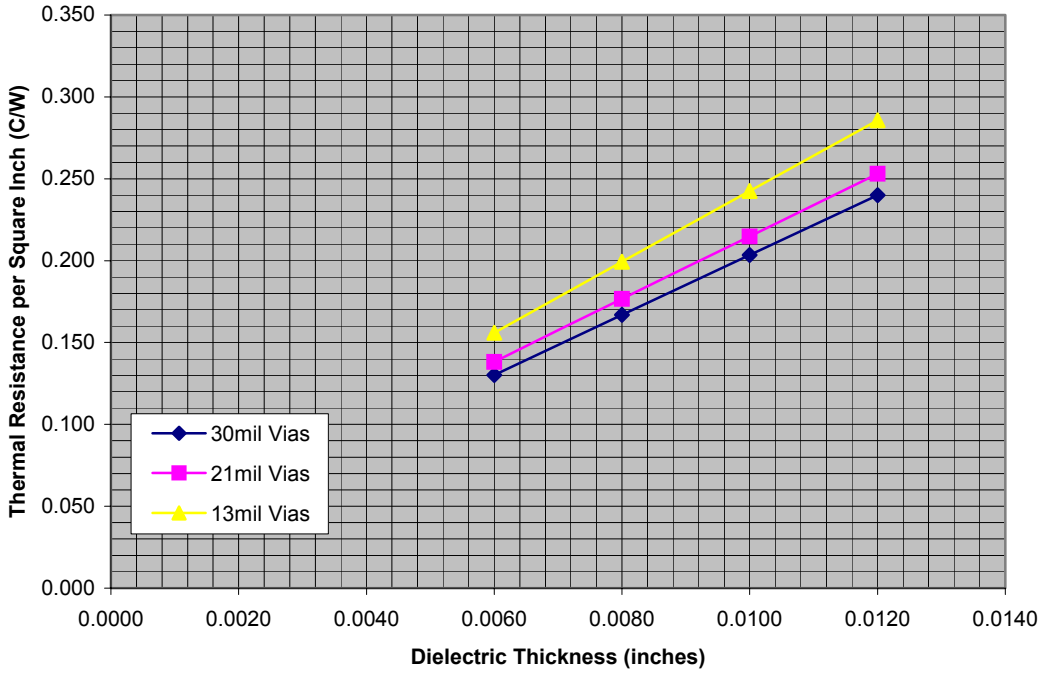

Figure 8.1d: Thermal Resistance vs 1KA Dielectric Thickness for 100mil Pitch, 2 oz foil with 1.4mil plating & delta T=50 C