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Qualification and Performance Specification for Rigid Printed Boards

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IPC-6012E

Qualification and Performance Specification for Rigid Printed Boards

Developed by the Rigid Printed Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) of IPC

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IPC-6012B with
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Amendment 1 - July 2000
IPC-6012A - October 1999
IPC-6012 - July 1996
IPC-RB-276 - March 1992

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC

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Qualification and Performance Specification for Rigid Printed Boards

1 SCOPE

1.1 Statement of Scope This specification establishes and defines the qualification and performance requirements for the fabrication of rigid printed boards.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of rigid printed boards based on the following constructions and/or technologies. These requirements apply to the finished product unless otherwise specified:

- Single-sided, double-sided printed boards with or without plated-through holes (PTHs).
- Multilayer printed boards with PTHs with or without buried/blind vias/microvias.
- Active/passive embedded circuitry printed boards with distributive capacitive planes and/or capacitive or resistive components.
- Metal core printed boards with or without an external metal heat frame, which may be active or non-active.

1.2.1 Supporting Documentation IPC-A-600, which contains figures, illustrations and photographs that can aid in the visualization of externally and internally observable acceptable/nonconforming conditions, may be used in conjunction with this specification for a more complete understanding of the recommendations and requirements.

1.3 Performance Classification and Type

1.3.1 Classification This specification establishes acceptance criteria for the performance classification of rigid printed boards based on customer and/or end-use requirements. Printed boards are classified by one of three general Performance Classes as defined in IPC-6011.

1.3.1.1 Requirement Deviations Requirements deviating from these heritage classifications **shall** be as agreed between user and supplier (AABUS).

1.3.1.2 Space Requirement Deviations Space performance classification deviations are provided in the IPC-6012ES Addendum and are applicable when the addendum is specified within the procurement documentation.

1.3.2 Printed Board Type Printed boards without PTHs (Type 1) and with PTHs (Types 2-6) are classified as follows and may include technology adders as described in Table 1-1:

Type 1 — Single-Sided Printed Board
Type 2 — Double-Sided Printed Board
Type 3 — Multilayer Printed Board without blind or buried vias
Type 4 — Multilayer Printed Board with blind and/or buried vias (may include microvias)
Type 5 — Multilayer metal core Printed Board without blind or buried vias
Type 6 — Multilayer metal core Printed Board with blind and/or buried vias (may include microvias)

1.3.3 Selection for Procurement Performance Class **shall** be specified in the procurement documentation.

The procurement documentation **shall** provide sufficient information to fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is to be in accordance with IPC-2611 and IPC-2614.

The procurement documentation **shall** specify the thermal stress test method to be used to meet the requirement of 3.6.1. Selection **shall** be from those depicted in 3.6.1.1, 3.6.1.2 and 3.6.1.3. If not specified (see 5.1), the default **shall** be per Table 1-2.

When tested in accordance with IPC-TM-650, Method 2.4.28.1, the maximum percentage of cured solder mask lifting from the G coupon or printed board **shall** be in accordance with Table 3-16.

Table 3-16 Solder Mask Adhesion

Surface	Maximum Percentage Loss Allowed		
	Class 1	Class 2	Class 3
Bare Copper	10	5	0
Gold or Nickel	25	10	5
Base Laminate	10	5	0
Melting Metals (Tin-lead plating, fused tin-lead, and bright acid-tin)	50	25	10

3.7.3 Solder Mask Thickness Any requirement for the measurement of solder mask thickness **shall** be AABUS. If a thickness measurement is required, instrumental methods may be used or assessment may be made using a microsection of the parallel conductors on the E coupon or Destructive Physical Analysis (DPA) (see 3.10.12, thermal stress not required). For additional guidance on solder mask thickness measurement options, see the IPC-6012 Automotive Addendum.

3.8 Electrical Requirements When tested as specified in Table 4-3 and Table 4-4, the printed boards **shall** meet the electrical requirements detailed in the following paragraphs.

3.8.1 Dielectric Withstanding Voltage Applicable test coupons or printed boards **shall** meet the requirements of Table 3-17, without flashover, or breakdown between conductors, or conductors and lands. The dielectric withstanding voltage test **shall** be performed in accordance with IPC-TM-650, Method 2.5.7. The dielectric withstanding voltage **shall** be applied between all common portions of each conductor pattern and adjacent common portions of each conductor pattern. The voltage **shall** be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. For embedded passive device capacitor materials, the dielectric withstanding voltage for adjacent plane layers that are not electrically common **shall** be per IPC-6017.

Table 3-17 Dielectric Withstanding Voltages

	Class 1	Class 2 and Class 3
Voltage for Spacing 80 µm [3,150 µin] or greater	No requirement	(500 +15 -0) V (dc)
Voltage for Spacing less than 80 µm [3,150 µin]	No requirement	(250 +15 -0) V (dc)
Time	No requirement	30 sec +3, -0

3.8.2 Electrical Continuity and Isolation Resistance Finished printed boards **shall** be tested in accordance with IPC-9252. Electrical continuity and isolation resistance testing of blind and buried structures is not required for in process checks.

3.8.3 Circuit/Plated Hole Shorts to Metal Substrate Printed boards **shall** be tested in accordance with 3.8.1 except that polarizing voltage of (500 +15 -0) V (dc) **shall** be applied between conductors and/or lands and the metal substrate (heat sink or core) in a manner such that each conductor/land area is tested (e.g., using a metallic brush or aluminum foil). The printed board **shall** be capable of withstanding (500 +15 -0) V (dc) between circuitry/plated holes and the metal core substrates. There **shall** be no flashover or dielectric breakdown.

3.8.4 Moisture and Insulation Resistance (MIR) Test coupons **shall** be tested in accordance with the procedure outlined below. The test coupon **shall not** exhibit subsurface imperfections in excess of that allowed in 3.3.2. Insulation resistance **shall** meet the minimum requirements shown in Table 3-18 (at (500 +15 -0) V (dc)). Non-component flush printed boards **shall** have a minimum requirement of 50 MΩ for all classes.

Table 3-18 Insulation Resistance

	Class 1	Class 2	Class 3
As received[1]	Maintain electrical function	500 MΩ	500 MΩ
After exposure to moisture	Maintain electrical function	100 MΩ	500 MΩ

Note 1. This measurement is taken after conformal coating material has been applied to the test coupon in accordance with IPC-TM-650, Method 2.6.3.

The moisture and insulation resistance for printed boards **shall** be performed in accordance with IPC-TM-650, Method 2.6.3. Conformal coating in accordance with IPC-CC-830 **shall** be applied to the external conductors prior to chamber exposure. Final measurements **shall** be made at room temperature within two hours after removal from the test chamber. All layers

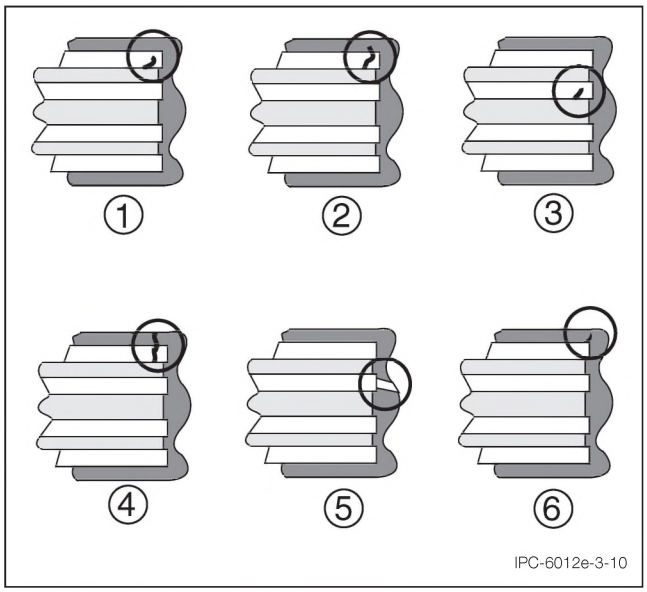

Figure 3-10 Copper Crack Definition[7]

Note 1. "A" cracks - crack in external foil.
Note 2. "B" cracks - crack does not completely break plating.
Note 3. "C" cracks - crack in internal foil.
Note 4. "D" cracks - complete fracture.
Note 5. "E" cracks - barrel crack in plating only.
Note 6. "F" cracks - corner crack in plating only.
Note 7: Copper plating as shown may include multiple plating layers or cap plating.

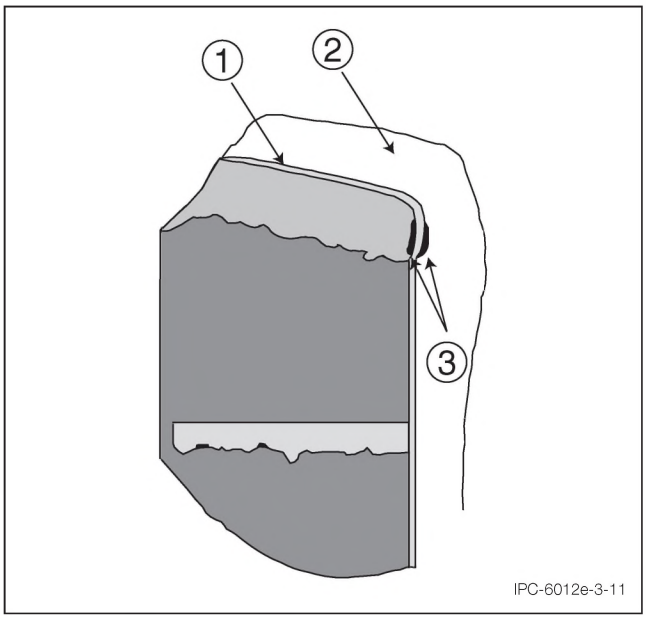

Figure 3-11 Separations at External Foil

Note 1. Conductive coatings.
Note 2. Electrolytic copper.
Note 3. Area of acceptable separation along the vertical edge of the external foil.

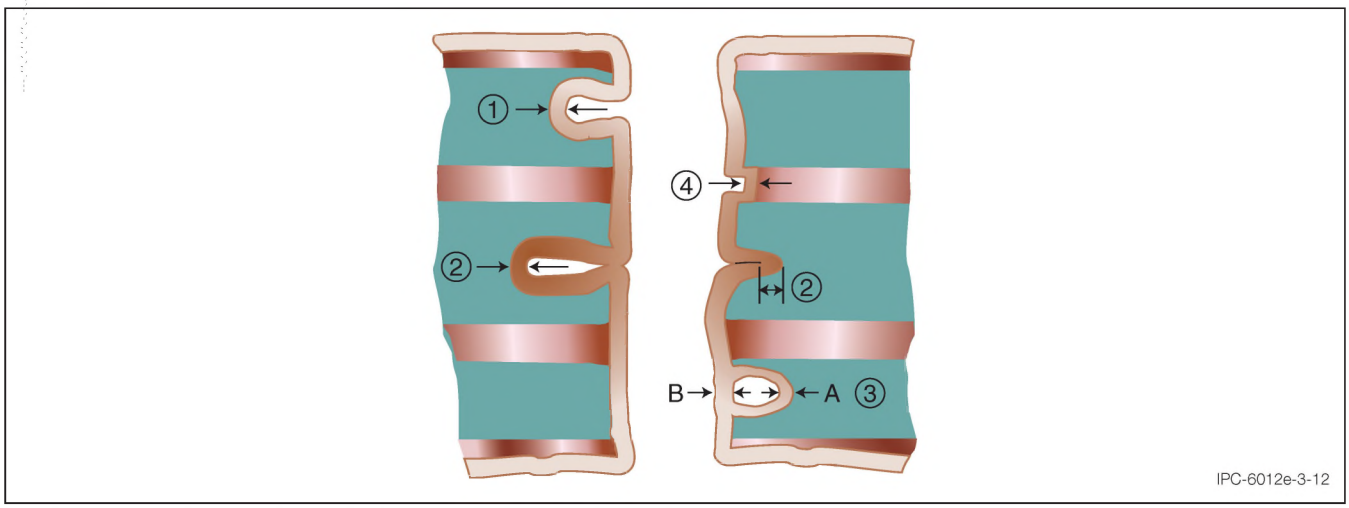

Figure 3-12 Plating Folds/Inclusions – Minimum Measurement Points

Note 1. Minimum copper plate measurement point. Plating folds that are not enclosed and where the minimum copper plate thickness in Tables 3-4, 3-5, or 3-6 is met are acceptable.
Note 2. Enclosed plating folds (inclusions) with demarcation line visible. Measure and accept per **Note 1.**
Note 3. Enclosed plating fold with no visible demarcation line. The thickness measurement A+B shall comply with the minimum copper plate thickness in Tables 3-4, 3-5, or 3-6.
Note 4. Minimum copper plate measurement point for negative etchback.

3.6.2.3 Laminate Voids For Class 2 and Class 3 products, there **shall** be no laminate voids outside of any thermal zones (see Figure 3-13) in excess of 80 µm [3,150 µin]. For Class 1 products, voids allowed outside of any thermal zone (see Figure 3-13) **shall not** exceed 150 µm [5,906 µin]. Boundary line voids that overlap into a thermal zone **shall not** be in excess of 80 µm [3,150 µin] for Class 2 or Class 3 products and 150 µm [5,906 µin] for Class 1 products. Multiple voids between two adjacent plated holes in the same plane **shall not** have a combined length which exceeds these limits. Voids between conductive patterns that are not electrically common in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.

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